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WHITE PAPER

USB 3.2: The Latest USB Type-C Challenge for SoC Designers

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Abstract

This white paper outlines applications that benefit from USB 3.2's increased bandwidth, describes the latest USB 3.2 specification for USB Type-C™, and explains how the latest specification affects speed using USB Type-C connectors and cables. Additionally, the white paper discusses USB 3.2 implementation, the new features of USB 3.2, and how designers can successfully integrate USB 3.2 IP in their next design.

USB 3.2 Applications

Many applications have an insatiable "need for speed." Mass storage is a classic example where minimizing the time spent waiting for file transfers greatly benefits consumers. Today most mass storage devices only connect at USB 3.0 speeds, which is faster than spinning hard disk drives (HDD). However, the rapid transition to flash based Solid State Disks (SSD) means USB 3.0 has become a bottleneck. USB 3.2 mass storage devices connected at 20Gbps offers more than four times the actual throughput of USB 3.0 and match the capabilities of the latest SSDs.

Graphics Adaptors

External USB graphics adapters can also take advantage of USB 3.2. USB 3.2 enables the use of long cables (up to 3m) at 10Gbps connection speeds or 20Gbps speeds for 1m cables, both with high resolution, high refresh rate, low compression, and multiple displays. Some docking stations simultaneously connect with both USB and DisplayPort, using one lane pair for USB and one or two lanes for DisplayPort. If the consumer needs more display capability, DisplayPort Alternate mode allows all four Type-C lanes to be used for DisplayPort; however, the USB connections are limited to USB 2.0 speeds.

Video Applications

Still and video cameras generate more data than can be moved in real time over a USB connection, so they use compression to reduce both throughput and storage requirements. Cameras often include mass storage functionality, which benefits from the higher USB 3.2 connection speeds.

In addition to standard consumer video applications, industrial vision systems can also take advantage of USB 3.2 speeds. In industrial vision systems, compression is normally not an option since image capture, processing, and taking appropriate actions, like removing an item from a high speed conveyor belt, is time-critical. Using USB 3.2 enables these systems to support higher resolutions or frame rates.

Automotive Applications

Automotive systems do not normally support USB 3.1 Gen 2 connections due to cable length and proprietary automotive connectors. However, because a USB 3.2 Gen 1x2 connection doubles throughput to 10Gbps compared to USB 3.1 Gen 1, infotainment data transfer could be significantly improved. In service mode, this speeds up infotainment system firmware and application updates, including map and navigation data. In mission mode, the consumer can connect any USB 2.0 or USB 3.x device and they will work due to USB backward compatibility standards.

USB 3.2 for Debug

Firmware engineers and software developers can utilize USB 3.2 to provide consumers with a high-quality product. More complex chips require more bandwidth for efficient Trace and Debug output. Dedicated Trace and Debug ports use expensive, dedicated capture boxes connected to dedicated development boards, typically only available to a few engineers. Synopsys USB Device Controllers or Dual Role Controllers in Device mode offer External Buffer Control (EBC) capability. EBC enables up to 20Gbps throughput for Trace and Debug data that is output from the product without software intervention after initial setup. The existing Type-C connector on the product, standard USB cables, and PCs/laptops are used to capture trace and debug data. Therefore, USB 3.2 and EBC provides advanced Trace and Debug capabilities for more engineers and developers, enabling them to develop better quality products faster.

Defining USB 3.2

The USB 3.2 specification replaces the USB 3.1 specification. USB 3.2 introduces a new nomenclature, just like the USB 3.1 specification introduced a new nomenclature when replacing the USB 3.0 specification. This means all new USB products supporting Enhanced SuperSpeed should be designed per the USB 3.2 specification regardless of the supported connection speeds.

USB 3.2 defines the following connection speeds:

- General nomenclature: Gen X x Y—(Speed x Lanes)
- Enhanced SuperSpeed Gen 1x1—(5G)
- Enhanced SuperSpeed Gen 2x1—(10G)
- Enhanced SuperSpeed Gen 1x2—(5G*2 =10G)
- Enhanced SuperSpeed Gen 2x2—(10G*2 =20G)

The maximum throughput after line encoding overhead is approximately 4Gbps, 9.7Gbps, 8Gbps, and 19Gbps for the four different USB 3.2 connection speeds. Actual throughput, after various USB protocol and device class overhead, is lower and implementation dependent.

Both USB 3.2 Gen 2x1 and Gen 1x2 provide a 10Gbps raw data rate. However, due to the more efficient line encoding for Gen 2, throughput for Gen 2x1 is approximately 1.2 times higher than for Gen 1x2. Both 10Gbps connection speeds are needed and support different use cases.

Mapping USB 3.2 nomenclature to USB 3.1 and USB 3.0 nomenclature:

- Gen 1x1 = SuperSpeed –> USB 3.0 –> USB 3.1 Gen 1
- Gen 2x1 = SuperSpeedPlus –> USB 3.1 –> USB 3.1 Gen 2

USB 3.2 marketing recommendations has not yet been published by USB-IF. Consumer confusion could be reduced with the consistent use of USB 3.0, USB 3.1, USB 3.2 10G, and USB 3.2 20G. Regardless of which marketing names are used to describe USB 3.2 products, it is important to be accurate and truthful with respect to which connection speeds a USB 3.2 product supports.

USB 3.2 and USB Type-C Cables and Connectors

USB has stayed relevant for consumers for more than 20 years by publishing continuous specification updates that increase speed, add functionality and ease of use, and preserve backward compatibility to earlier USB specifications. Designers working on new products should refer to the USB 3.2 specification, which was released in September 2017. The specification doubles the connection speed of USB 3.1, providing up to 20Gbps using USB Type-C connectors and cables.

USB Type-C is the current standard USB connector used in most new Host (PCs, laptops, 2-in-1, convertibles, hybrids), and Dual Role (tablets, phones) Devices. Type-C peripherals are common and Type-C chargers, mini docking stations, A/V adapters, hubs, and more are readily available. The USB-IF is emphasizing the transition to a USB Type-C connection standard within the USB 3.2 specification by moving the USB cable and connector chapter to a separate document and renaming the standard-A, standard-B, and mini/micro connectors as legacy USB connectors.

USB 3.2 Dual Lane mode is designed for use with USB Type-C connector. USB 3.2 takes advantage of the four differential SuperSpeed/SuperSpeedPlus pairs present in the USB Type-C connector, unlike USB 3.1 and USB 3.0 which used one or the other TX/RX lane pair, depending on Type-C connector orientation.

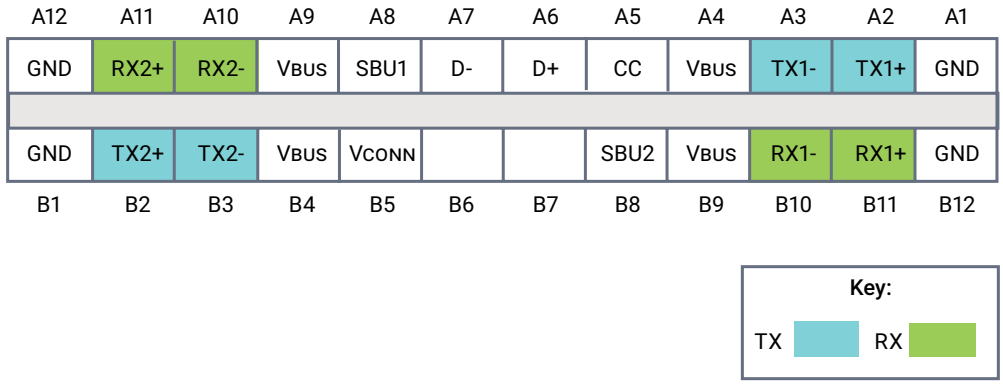

Figure 1: USB Type-C receptacle with four differential pairs/lanes (Source: USB Type-C Specification Figure 2-2)

All passive USB Type-C cables can be used for USB 3.2 Gen Xx2 connections since four SuperSpeed/SuperSpeedPlus differential pairs are mandatory per the USB Type-C specification. A passive cable designed for Gen 2 (10G) is limited to approx. 1m length and can support the new 20G connection speed. Two- to three-meter passive cables designed for Gen 1 (5G) can support the new 10G connection speed.

Active cables are used to extend USB Type-C cable length beyond 1m for Gen 2 and up to 5m for Gen 1. Some active cables might have chosen to not support four differential pairs. Also, active cables designed for DisplayPort Alternate mode could be designed in a way that does not support USB at all. USB-IF (USB) and VESA (DisplayPort) are defining active cable specifications to ensure that active cables will work with USB 3.2 connections.

USB 3.2 implementations achieve a 20Gbps raw data rate by lane striping and lane bonding (e.g., splitting and combining data) from two USB 3.1 (10G) lanes. USB 3.2 also supports 10Gbps by striping and bonding two USB 3.0 (5G) lanes. USB 3.2 also supports USB Type-C features like Alternate Modes, Power Delivery, and Digital Audio.

USB 3.2 backward compatibility requirements means USB 3.2 system design and operation is non-trivial. USB 3.2 Host controllers must support all USB Devices and connection speeds. This means USB 1.1, USB 2.0, USB 3.0, USB 3.1 and USB 3.2 Devices can be connected to a USB 3.2 Host. USB 3.2 Gen Xx2 dual-lane operation is only possible when the Host controller and the connected hubs and/or peripherals are USB 3.2 Gen Xx2 capable.

USB 3.2 Devices must support connections to any USB Host, and fall back to single lane mode (Gen Xx1) if connected to a USB 3.0 or USB 3.1 Host. Likewise, a USB 3.2 Host will fall back to single lane mode when USB 3.0 or USB 3.1 hub is connected. A USB 3.2 hub will fall back to single lane mode if connected to a USB 3.0 or 3.1 Host.

A USB 3.2 hub connected to a USB 3.2 Host must support all variants of downstream peripheral devices and convert between single-lane and dual-lane as needed. USB 3.2 hubs must support store and forward handling of packets and speed conversion. Designing a compliant USB 3.2 hub is quite complicated.

Figure 2 illustrates USB 3.2 lane striping and lane bonding: In USB 3.2 Gen Xx2 mode, the host and device controller TX paths run at twice the speed of a single-lane USB 3.1 or 3.0 connection. Payload data is split (striped) across two TX/RX lanes in the PHY and cable, and combined (bonded) in the Device and Host controller RX paths.

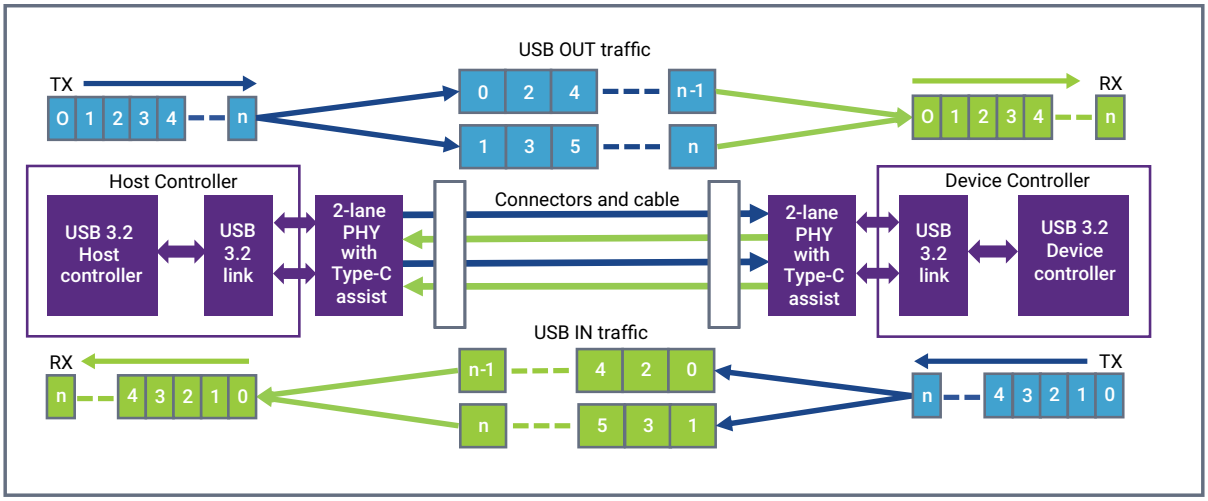

Figure 2: USB 3.2 lane striping and lane bonding

The USB 3.2 specification renamed the standard USB connectors as Legacy USB connectors. Legacy cable assemblies and Type-C to legacy adapter cables only support single-lane operation and are not applicable for USB 3.2 Gen Xx2 connections.

System-on-chip (SoC) integrators using USB 3.2 IP must be aware of the increased bandwidth and low latency required to enable the 20Gbps raw data rate. A minimum of 2Gbytes/s sustained Read and Write bandwidth are required between USB controller and system memory to implement USB 3.2. Latency requirements can be relaxed by adding FIFO and pre-fetch capability to the USB 3.2 controller. Choosing the right USB 3.2 Host, Device or Dual Role controller simplifies SoC or ASIC IP integration, reduces risk, and accelerates time-to-market.

USB 3.2 Controller

Changes are required to the link layer of USB 3.0 or USB 3.1 controller to support USB 3.2 Gen Xx2 operation. During Polling. PortMatch, the Host and Device discover and negotiate the single lane verses dual lane capability. The USB 3.2 connection priority is Gen 2x2, with fallback to Gen 2x1, then Gen 1x2, and finally Gen 1x1.

USB 3.2 link setup is performed on the configuration lane, which is defined as the lane that would have been used for a Gen Xx1 connection. Low frequency signaling is exchanged only on the configuration lane. Receiver termination detection is only required on the configuration lane. However, ordered sets are transmitted simultaneously on both lanes. Gen Xx2 traffic is striped across two lanes, with alternating 8b/10b symbols for Gen 1x2 connections and alternating Bytes for Gen 2x2 connections using 128b/132b encoding. Minimal lane skew is required to properly combine or 'bond' the two separate lanes.

To maximize throughput, a USB 3.2 Host controller must implement USB 3.2-aware schedulers. In particular, the periodic transfer scheduler must be designed to manage multiple USB 3.0, 3.1, and 3.2 devices that are connected to hub ports at 20Gbps, 10Gbps, 2*5Gbps, and 5Gbps connection speeds.

Software Stacks

Just as the USB 3.1 programming model did not change from USB 3.0, the programming model for USB 3.2 Host and Device controllers does not change to support x2 connections. USB 3.0, USB 3.1, and USB 3.2 xHCI compliant Host controllers all use the same xHCI Host software stack. Synopsys' USB Device Controller uses the same Device software stack for USB 3.0, USB 3.1, and USB 3.2. However, 20Gbps throughput can reveal operating system and/or CPU and memory bottlenecks that were not present at 5Gbps or 10Gbps. Also, Device class drivers and/or Device functions like mass storage, networking, and video might need to be optimized to take advantage of the new 20Gbps connection speed.

USB 3.2 PHY

Single-lane Type-C PHYs use analog multiplexers to route the active TX/RX lane pair for Gen Xx1 connections. Analog multiplexers degrade signal quality and are not preferred for Gen 2 operation. Single-lane Type-C PHYs cannot support USB 3.2 Gen Xx2. An alternate Type-C PHY implementation has two independent RX/TX lane pairs and uses a digital crossbar to enable one or the other lane for Gen Xx1 connections. A two-lane PHY can be modified to have one or the other lane active for Gen Xx1 and both lanes active for Gen Xx2, shown in Figure 3.

Mode	Type-C Pin Name	TX1 +/- A2/A3	RX1 +/- B11/B10	TX2 +/- B2/B3	RX2 +/- A11/A10	Connector orientation
	PHY lane configuration	USB TX	USB RX	USB TX	USB RX	PHY lane configuration
		or DP TX	or DP TX	or DP TX	or DP TX	
	USB 3.1 only	SS/SS+	SS/SS+	Not used	Not used	Type-C normal
		Not used	Not used	SS/SS+	SS/SS+	Type-C flipped
	USB 3.2 only	SS/SS+ lane 0	SS/SS+ lane 0	SS/SS+ lane 1	SS/SS+ Lane 1	Type-C normal
		SS/SS+ lane 1	SS/SS+ lane 1	SS/SS+ lane 0	SS/SS+ Lane 0	Type-C flipped
	USB and DP (1,2 lanes)	SS/SS+	SS/SS+	DP main lane 1	DP main lane 0	Type-C normal
		DP main lane 1	DP main lane 0	SS/SS+	SS/SS+	Type-C flipped
	DP only (1,2,4 lanes)	DP main lane 2	DP main lane 3	DP main lane 1	DP main lane 0	Type-C normal
		DP main lane 1	DP main lane 0	DP main lane 2	DP main lane 3	Type-C flipped

Key: TX RX DP

Figure 3: USB 3.2 and DisplayPort (DP) Alt Mode Lane usage on Type-C connector

Synopsys USB Type-C PHYs are being developed in multiple process nodes for USB 3.2 and USB/DisplayPort applications. Synopsys USB-C PHYs use Type-C Assist (TCA) with digital cross-bar switch. This architecture ensures the best possible signal quality, providing a reliable consumer experience. Developers can integrate Synopsys USB Type-C PHYs and controllers in ASICs or SoCs in the process node that are most suitable for their designs.

USB 3.2 Subsystem and Solutions

For USB 3.2 designers, Synopsys offers controller and PHY IP. Using these IP, designers add the required interconnections, wrappers, clock, reset, test, debug and scan circuitry when designing their ASIC or SoC. However, integrating customized subsystems (Figure 4) reduce risk and integration effort and accelerate time-to-market. Integrating a subsystem allows designers to concentrate on their own value-add activities.

For example, a DesignWare USB Type-C/DisplayPort Subsystem can include a USB 3.2 Dual Role Device Controller, DisplayPort 1.4a TX Controller, HDCP 2.2 Embedded Security Module, and USB-C/DisplayPort, USB 2.0 and DP AUX PHYs. The subsystem includes all required interconnections, wrappers, and Verification IP to validate the operating modes shown in Figure 3.

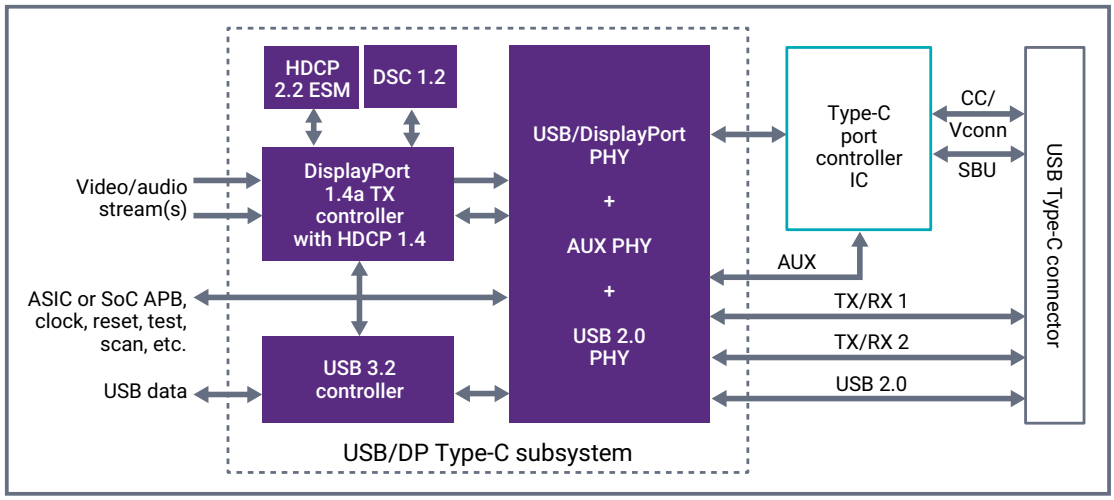

Figure 4: DesignWare Interface IP Subsystem Block Diagram

USB 3.2 Prototyping for InterOp and Compliance

A major part of modern IP development is 'virtual.' IP designers use simulations and verification IP to validate a design before releasing RTL code to system designers for integrating in their ASIC or SoC. System designers can use virtual IP prototyping services to validate SoC integration and develop firmware and software. However, IP designers and system designers need a hardware prototype implementation for SW development, demos, interoperability testing, debug, and compliance testing.

Synopsys uses HAPS-80 FPGA-based prototyping systems for USB 3.2 IP controller development. A USB 3.2 test chip on a PHY daughterboard connects to the FPGAs in the HAPS-80 system. Both USB 3.2 Host and Device controllers are prototyped. Figure 5 shows the PHY board and device controller with a standard mass storage function implemented on a Linux PC.

The device controller connects to another HAPS-80 system and PHY board that implements a USB 3.2 Host controller. The Host controller is connected to a standard PC running Windows 10, using the standard xHCI software stack.

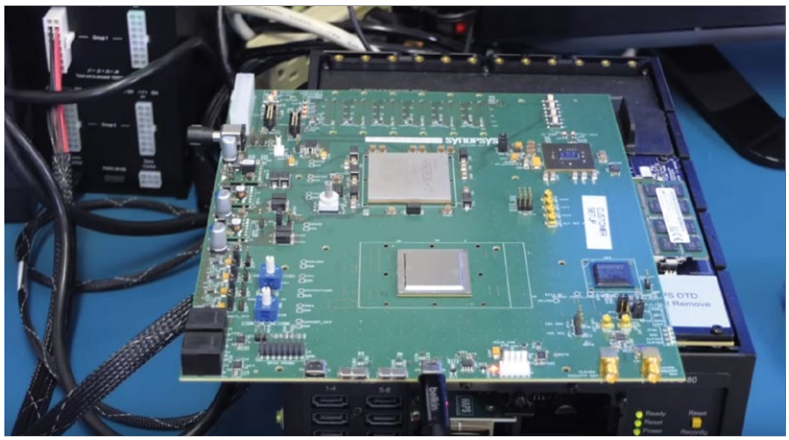

Figure 5: Synopsys HAPS-80 FPGA-based prototyping system used to develop and test USB 3.2 IP

Synopsys and USB 3.2

Synopsys is a major contributor to USB technology and standards, and the world's most preferred and most widely used supplier of USB IP for all USB standards. Contact Synopsys for further information on how we can help your next ASIC or SoC design support the latest USB 3.2 specification.

USB 3.2 Resources:

- Video: http://bit.ly/usb32demo_video
- Blog post: http://bit.ly/USB32Blog
- Blog post: http://bit.ly/butwhyusb32_blogpost
- USB 3.2 specification bundle: http://www.usb.org/developers/docs
- USB Developer Days presentations: http://www.usb.org/developers/presentations/

08/16/18.CS260381732_USB 3.2_ USB Type-C Challenge for SoC Designers_WP.

Pub: Aug. 2018