iVerifier 2017.01

Release Notes

XPEEDIC 芯禾科技

ACCELERATE YOUR IC DESIGN

1. OVERVIEW

Xpeedic iVerifier solution provides designers a quick way to verify PDK models in Cadence Virtuoso environment. It includes two flows, one is schematic based and the other is layout based. In iVerifier schematic flow, the PDK model test bench is run in ADE with Spectre simulator by sweeping the CDF parameters of the PDK model. In iVerifier layout flow, Xpeedic full-wave EM solver IRIS is run by sweeping the geometry parameters of PCell. iVerifier provides a quick way to analyze and visualize the results, which helps PDK engineers or IC designers to assess the model quality.

The Release Notes cover the following releases:

iVerifier 2017.01

Release Date: April 13, 2017

The Release Notes present the latest information about iVerifier Version 2017.01 in the following sections:

2. SUPPORTED OPERATION SYSTEMS

iVerifier 2017.01 is available on 64bit Linux. Obtain the appropriate binary executable files for your operation system. The supported platforms for this release includes:

- SuSE
- RHEL5
- RHEL6

3. NEW FEATURES AND ENHANCEMENTS IN IVERIFIER 2017.01

iVerifier 2017.01 provides new features and enhancements as described in the following sections.

3.1 Usability Improvements

- Verify PDK models on Candence Virtuoso platform.
- Sweep geometry parameters of passive pcell.

3.2 Mesh improvements

- Replace via array or via bar with one line when merge via in order to improve solver performance.
- Mesh refine when singular triangle existing to achieve better convergence.
- Metal-to-Metal mesh support.
- Support via with hole inside.

3.3 Solver improvements

- Multi-frequency sweep plan support.
- Frequency and temperature dependent materials support.
- Metal-to-Metal simulation support.

3.4 Post-Processing improvements

- PLTS like grid mode support.
- TDR calculator.

- Delay and Skew calculator.
- Move marker along the line.