Seven Steps to an Accurate Worst-Case Power Analysis using the Xilinx Power Estimator

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Summary

Power and thermal specifications for FPGAs, MPSoCs, and RFSoCs must be determined in the early stages of a product design cycle, often even when the register transfer level (RTL) description is incomplete. The Xilinx® Power Estimator (XPE) can be used during the pre-design and pre-implementation stages of the design cycle for power analysis.

With the increasing complexity and compute power of modern programmable devices, an early analysis of power and thermal specifications is a must for a successful product design. The ability to estimate power consumption in a design is imperative for efficient part selection, board design, and system reliability. An accurate worst-case analysis early on helps you avoid the pitfalls of over designing or under designing the power or thermal portions of your system. This application note describes a seven-step procedure for analyzing the power requirements of your design using the Xilinx Power Estimator (XPE) spreadsheet tool.

Introduction

As a necessary step in any board design, power and thermal specifications need to be properly set to create a functioning and reliable system. In most cases, these power and thermal specifications should be set prior to PCB design and, due to the flexibility of Xilinx devices, often the FPGA, MPSoC, or RFSoC design is not complete or not even started prior to system design and/or PCB fabrication. This presents an interesting challenge for system designers, because power and thermal characteristics can vary dramatically depending on the bitstream (design), clocking, and data put into the device. Underdesigning the power or thermal system can make the device operate out of specification, which could result in the device not operating at the expected performance or potentially other more serious consequences including reliability and lifetime degradation. Overdesigning the power or thermal solution is generally less serious (although not desirable) because it can add unnecessary cost, size, weight, complexity, and potential time to the overall device design.

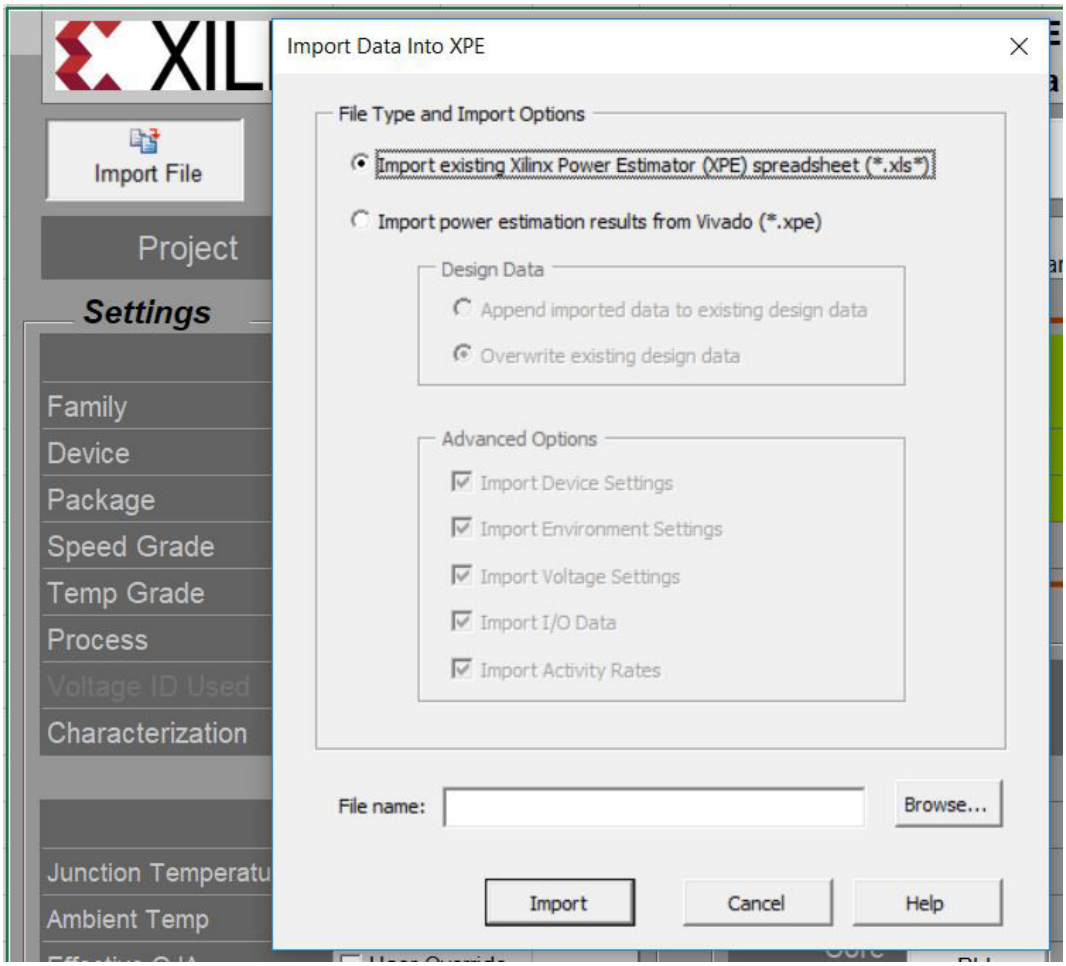
Prior to completing a design, power estimation is not trivial. The purpose of this application note is to simplify this task by splitting it into seven steps to achieve accurate worst-case power estimation prior to design completion and is primarily focused on power analysis.

Step 1: Updating to the Most Current XPE Version

Obtain the latest version of the Xilinx® Power Estimator (XPE) for the selected target device. It is important to make sure you are using the latest version of the XPE tool because power information is updated periodically to reflect the latest power modeling and characterization data. See the Xilinx Power Estimator (XPE) spreadsheet tool.

It is also helpful to check this web site occasionally during the design process to determine whether a newer version is available. You can import the data from a previous version of XPE using the updated XPE by selecting the **Import File** button on the Summary tab. Keeping XPE updated enables your design cycle to have the most accurate power information for system power analysis.

Figure 1: **Importing an Existing XPE Sheet**

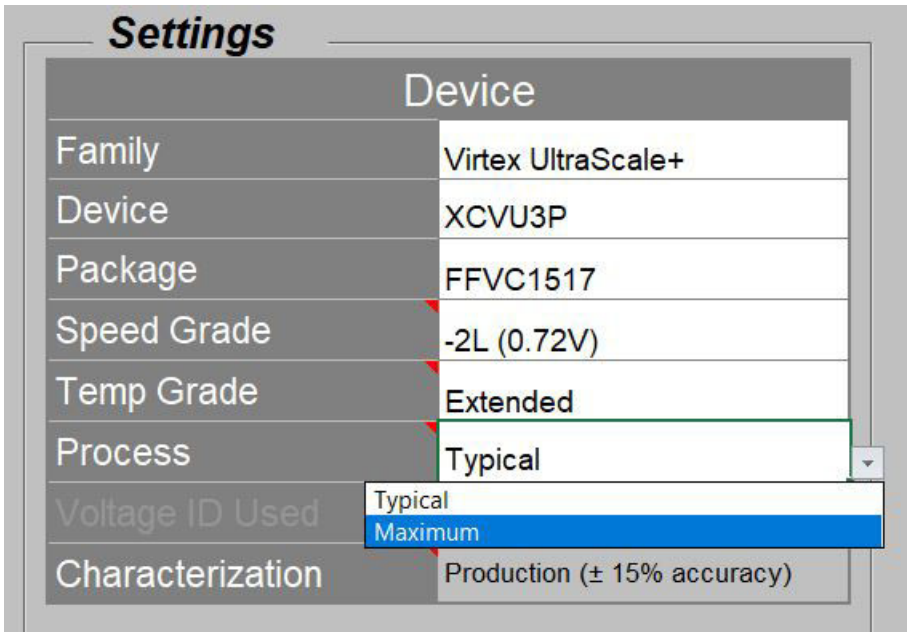


Step 2: Complete the Device Information on the Summary Tab

Make sure to set each field in the **Device** section of the Summary tab because each field can have a significant effect on the final power calculation, particularly the static and clocking power. The following steps describe the choices in the tool.

Figure 2: **Device Information—Summary Tab**

1. Select **Family**: Choose the appropriate family from the drop-down menu. XC, XA, and XQ families are available.
2. Select **Device**: Choose the smallest device that meets your requirements. An improperly chosen device can lead to incorrect static and dynamic power estimations such as the dynamic power reported for clocks and logic. An incorrect device setting can also result in improperly reported available resources.
3. Select **Package**: The package selection can affect the heat dissipation and the end junction temperature of the chosen device. An incorrect junction temperature can result in an incorrect static power calculation. The package selection also impacts the maximum current specification and a notification is triggered when the maximum is exceeded. Certain Xilinx device families are available in lidless packages (denoted by an S or B in the package name), these offer the lowest thermal resistance to the user thermal solution, the junction temperature of *any* device depends on your thermal solution. The only way to understand the effectiveness of the thermal solution in the end environment is to run a thermal simulation. Xilinx provides DELPHI thermal models for Siemens FloTHERM and Ansys Icepak. These models are available for download on the Xilinx website under the Device Models tab.
4. Select **Speed Grade**: Choose the appropriate device speed grade for your design. Some devices are offered at a lower V_{CCINT} voltage operation. The factors to consider when choosing these devices include reduced performance and lower power. These devices are indicated in the tool as -2L (0.72V) or -1L (0.72V).
5. Select **Temp Grade**: Choose the appropriate temperature grade for the device. Typically, the selection is **Commercial**, **Extended** or **Industrial**. This setting allows for the proper display of junction temperature limits for the chosen device. Some devices offer an excursion temperature operation, which raises the upper temperature operating limit to 110°C for a limited period. Refer to *Extending the Thermal Solution by Utilizing Excursion Temperatures* (WP517) for further information.
6. Select **Process**: For the purposes of a worst-case analysis, the recommendation is to set the process to **Maximum**. While the default setting of (**Typical**) results in a statistically accurate measurement, by changing the setting to **Maximum** the power specification is modified to worst-case values. Setting the **Maximum** process makes sure that the power and thermal delivery solution will work with any device that will be shipped.



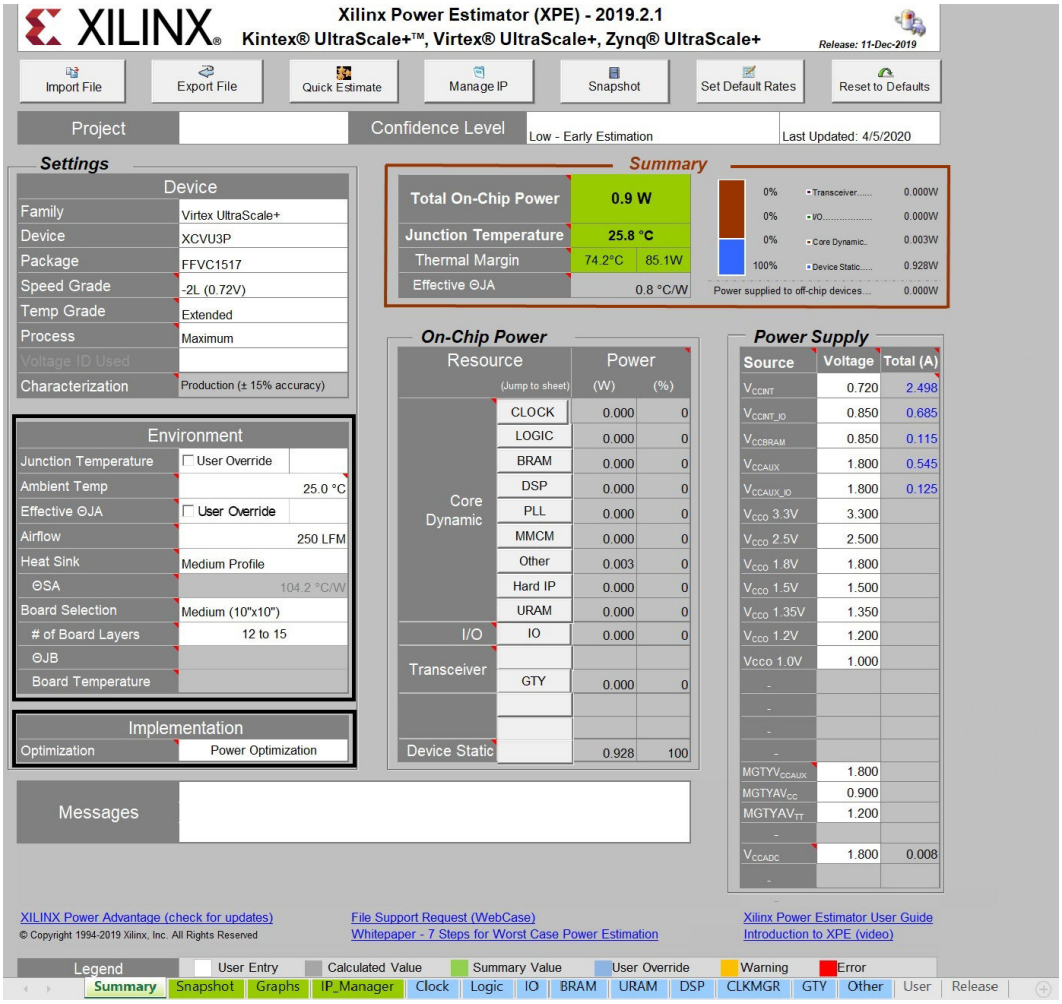
7. **Characterization**: This read-only field shows you the characterization level of the data, the % error for each of the characterization level is as follows:
   - Preview (±30% accuracy)
   - Advance (±25% accuracy)
   - Preliminary (±20% accuracy)
   - Production (±15% accuracy)

TIP: *The characterization accuracy level describes the accuracy of the model within XPE. The accuracy of the estimation depends on the accuracy of the information added by the user.*

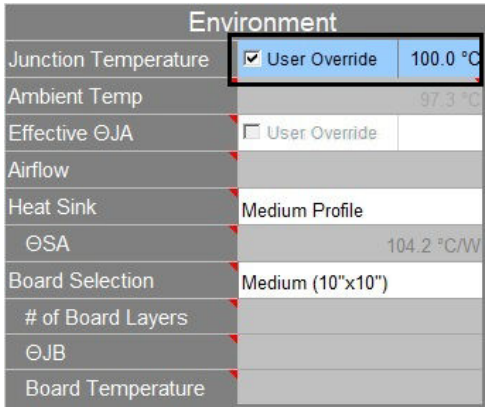
Step 3: Complete the Environment and Implementation Information on the Summary Tab

Set the proper thermal conditions in the environment section because they are important when calculating static power.

Figure 3: **Environment and Implementation Information – Summary Tab**



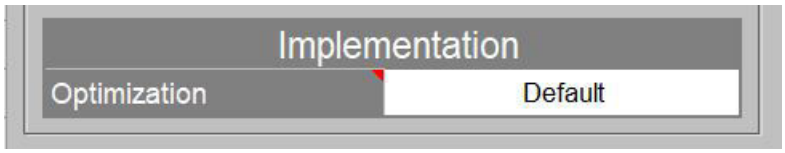
1. Set **Junction Temperature**: This field is used to force the device junction temperature to a specific value. For worst-case analysis, select **User Override** to change the maximum T_J, which is 100°C for the E and I temperature grade devices. With the process set to **Maximum** and the maximum T_J allowed for the temperature grade, the worst-case power is determined and the thermal design deploys an adequate thermal solution. When a low power design is required, improving the thermal solution further to reduce T_J will directly reduce power by lowering the static power component. For low-power designs and to improve power consumption, target a temperature below the maximum T_J.



Overriding the Junction Temperature causes all the fields to be grayed out (except the Heat Sink and Board Selection fields). Use Ambient Temp and Effective ΘJA when the values are derived from thermal simulations.

RECOMMENDED: *While there are additional environmental settings available, Xilinx recommends performing a thermal simulation to determine the Effective ΘJA. Xilinx provides DELPHI models for FloTHERM and Icepak at Downloads.*

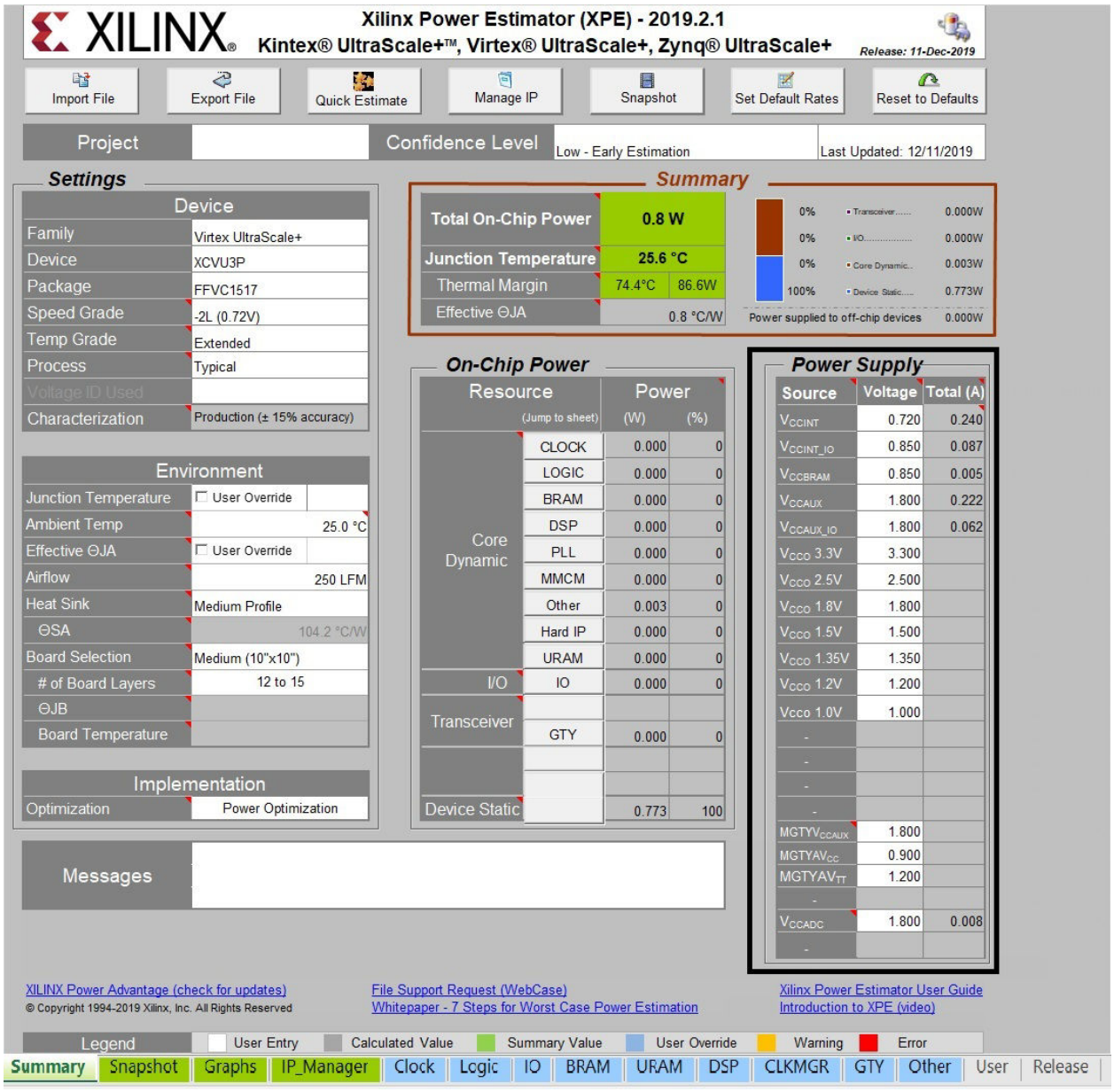
2. Set **Power Optimization**: Set the power optimization to **Default** to be inline with the default Vivado® Design Suite option. The following image shows the default power optimization setting for worst-case analysis in the Xilinx Power Estimator.



Step 4: Set Worst-case Voltage on All Supplies

By default, each voltage rail for a device is set to its nominal value in the Xilinx Power Estimator tool. To get a worst-case power estimation, the maximum DC offset of the regulator (in general is 1% higher) need to be specified. If you are not using some of the V_{CCO} or MGT voltage sources, keep the default values in those source specific rows.

Figure 4: **Power Supply Settings in the Xilinx Power Estimator Tool with Maximum Voltage Settings**

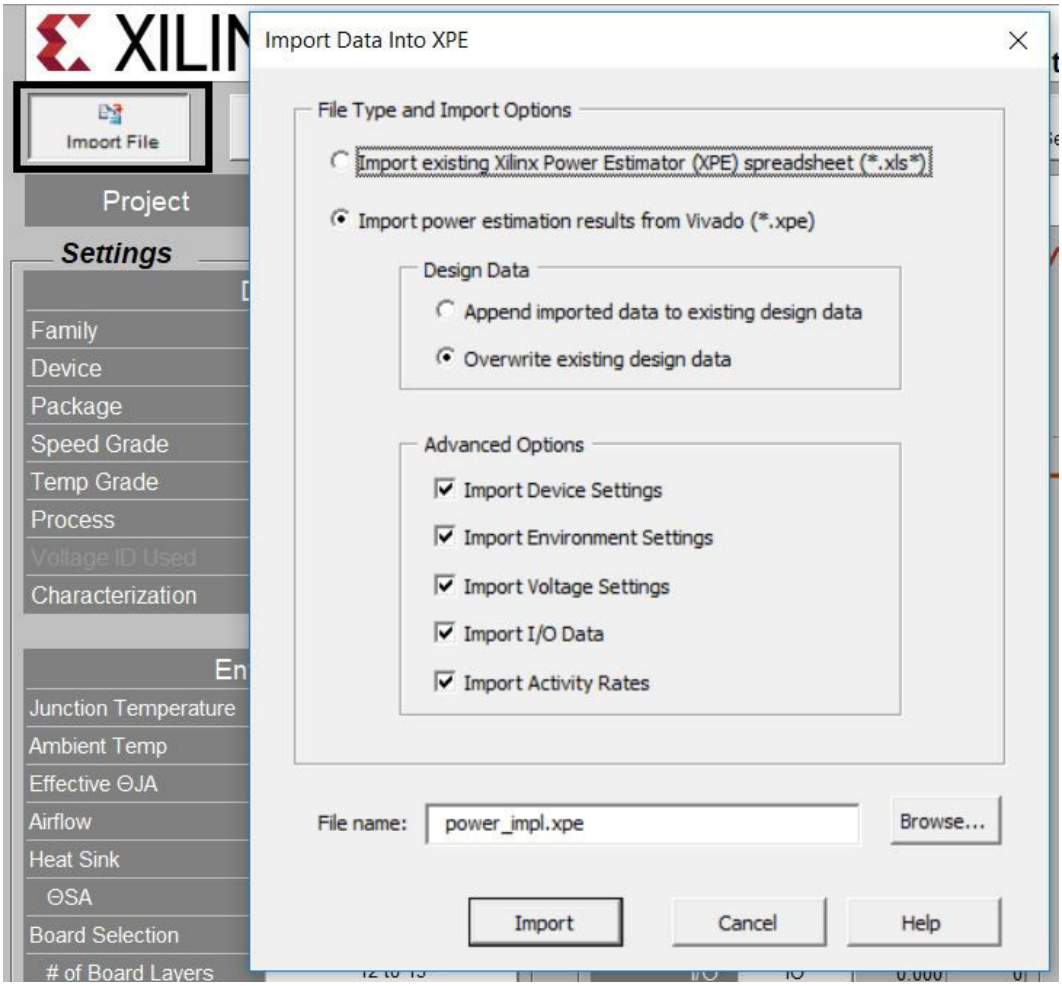


TIP: *Use nominal voltages for power delivery design. This allows for enough margin (positive and negative) to design an appropriate power supply. If the maximum or minimum levels are used, ANY ripple on the supplies could mean a violation of the operating specifications.*

Step 5: Enter Clock and Resource Information

If your design has already been through the Vivado tools or a previous revision of the design was run, those versions are a good starting point for the analysis. The output file (`*.xpe`) from Vivado Report_Power can be imported into the Xilinx Power Estimator tool to help fill out clock and resource information. To do this, use the Import File option located in the Summary tab of the Xilinx Power Estimator tool.

Figure 5: **Importing Vivado Report Power Output File into the Xilinx Power Estimator Tool**



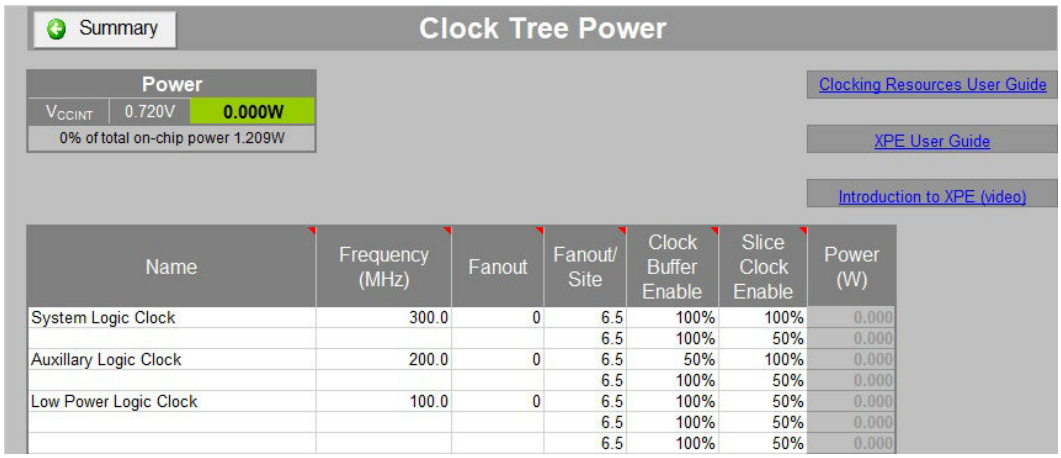
After importing the `*.xpe` file, additional information and adjustments are often needed to create a complete estimation. For each of the resource tabs, fill out the expected resources to be used in the design. Refer to *Xilinx Power Estimator User Guide* (UG440) for detailed information on specific fields in the individual tabs.

TIP: *When starting a new estimation, using a previous design that was correlated with hardware is the best starting point to give accurate toggle and switching rates.*

Clock Tree Power

Enter the various clocks and their frequencies in individual rows. For dynamic power calculations, the important factors to consider are activity and load capacitance being switched by each clock network in the design. Some factors for determining load capacitance are fanout and wire length. Typically, clock nets have higher activity and fanouts, which makes the values entered important. Fanout is managed in Step 6. During early power estimation calculations, the default Fanout/Site value is recommended. For imported `*.xpe` files, the fanout value is provided by Vivado and is based on the place and route results used to improve clock power accuracy.

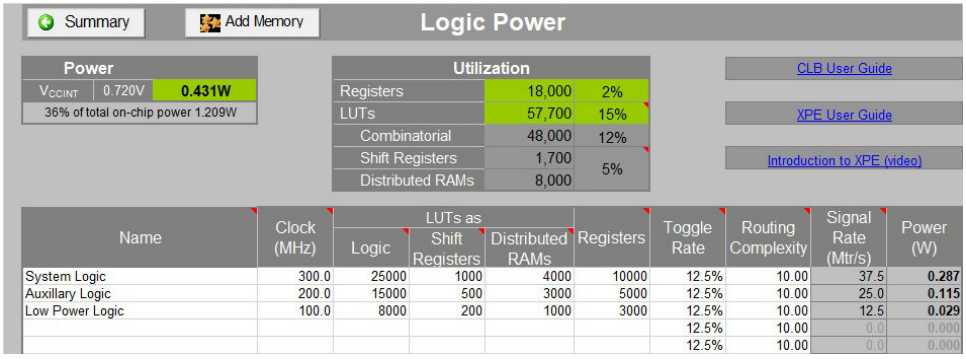
Figure 6: **Clock Tree Power Tab**



Logic Power

Use this tab to enter an estimate for the number of LUT resources configured as Logic, Shift Registers, and Distributed RAM Registers used in the design. Use the Add Memory button to simplify adding distributed memory to the design. Use different rows to separate the logic based on the clock domain they operate in. In the absence of a better estimate for you design, leave the Toggle Rate and Routing Complexity at the default values.

Figure 7: **Logic Power Tab**



During the early stages of design, it can be difficult to get accurate numbers for these resources. It is best to work with large round numbers that are close to a realistic estimation. A good practice is to consider the data entered into the Xilinx Power Estimator tool early as a constraint to the design. If you specify 25,000 LUTs for a portion of the design, then pay attention to that portion to be sure it stays within budget. If it grows beyond the initial power margin budget, then it is possible to take early action in the design. By making the budget parameters less of a guessing game and more of a guidance for the design, the early resource estimates are more controllable. If the design has an earlier revision, use it as the starting point by using the Import feature to populate the fields and build upon that base design.

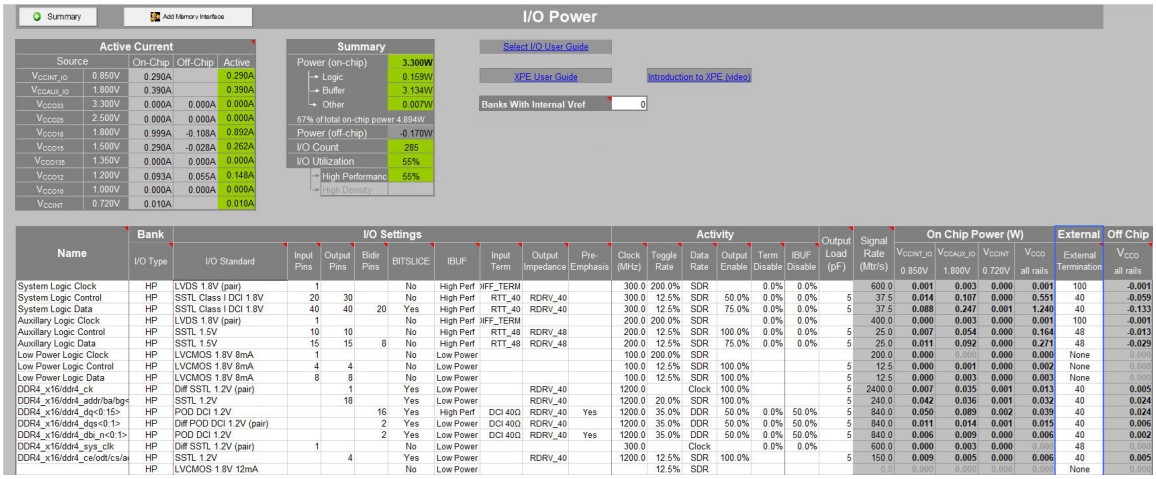
TIP: *When entering the clock frequency information, use the capabilities of Excel to relate that cell to the cell populated in the Clock Tree Power tab. To do this, select the desired* ***Clock (MHz)*** *cell in the logic view, type =, and select the cell in the* ***Clock Tree Power*** *tab corresponding to the clock source for that logic. The cell is populated with the value in the Clock Tree Power tab. The primary benefit of this methodology is that if the clock frequency is ever changed, either by a specification or when exploring power trade-offs vs. frequency, the value is only updated in one place and can be reflected throughout the Xilinx Power Estimator tool. This methodology can also reduce the chance of errors and inconsistencies during the data entry.*

I/O Power

With faster switching speeds and higher capacitive loads, I/O power can be a substantial part of the total power consumption of the device. Therefore, it is important to accurately define and fill in the I/O related parameters to get an accurate overall estimation of all rails of the device. Depending on the selected I/O standard and I/O circuitry, a significant amount of power can be consumed not only in the V_{CCO} rail but also the V_{CCINT} and V_{CCAUX} rails. By specifying each device interface separately and breaking out the interface signals to the data, control, and clock signals, it is easier to provide different I/O standards as well as other I/O characteristics, such as load and toggle rates.

TIP: *Use the Add Memory Interface button to add a memory interface into the I/O spreadsheet.*

Figure 8: **I/O Power Tab**



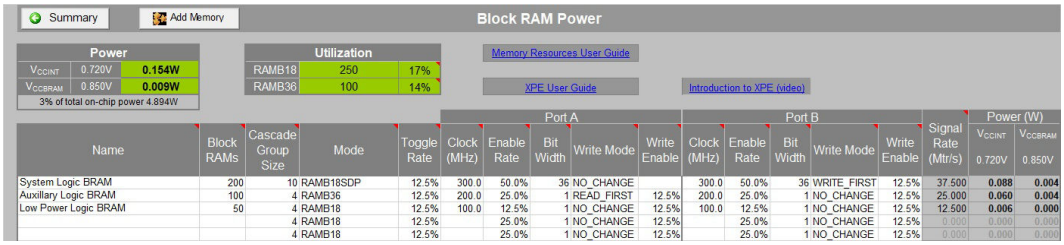
Differential pins are defined in pairs and are specified as a single entry. For example, if there is one differential input signal and four differential output signals using the LVDS 1.8V I/O standard, enter a 1 in the input column and 4 in the output column for that module name.

Block RAM Power

To set the number of block RAMs to be used in the design and the configuration and to accurately set the block RAM parameters, a good understanding of device resources and configuration possibilities is recommended. Make sure to adjust the **Enable Rate** for Port A or Port B because the amount of time the RAM is enabled is directly proportional to the dynamic power it consumes. Entering the proper value for this parameter is important for an accurate block RAM power estimation.

Use the Add Memory button to add the various types of block RAMs with the required configurations as rows in the Block RAM spreadsheet. Refer to the Using the Block RAM spreadsheet in the *Xilinx Power Estimator User Guide* (UG440) for guidelines.

Figure 9: **Block RAM Power Tab**

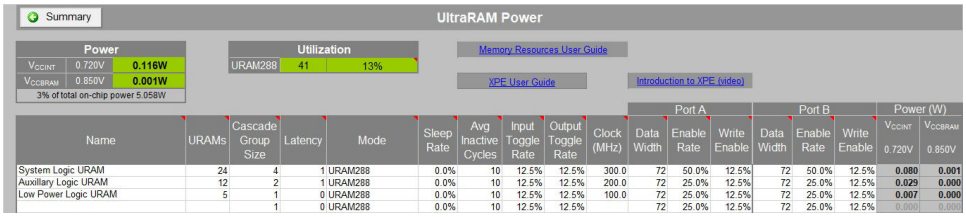


UltraRAM Power

UltraScale+™ devices support a high-density 288 Kb memory block (UltraRAM) that coexists with the block RAMs and enables deeper memory implementation. Dedicated routing in an UltraRAM column enables the entire column height to be connected.

Set the number and configurations of the URAM with attention to the **Enable Rate** for Port A or Port B because it is directly proportional to the dynamic power it consumes.

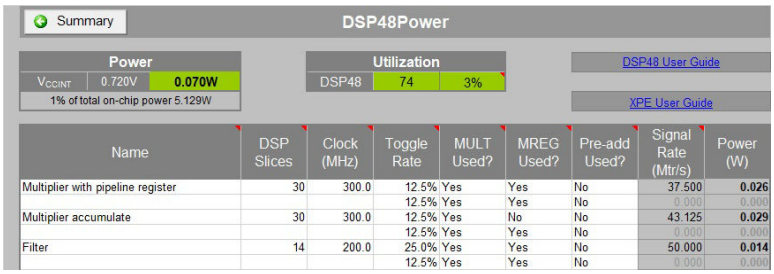
Figure 10: **UltraRAM Power Tab**



DSP48 Power

Complete the DSP48 Power tab with the required details. DSP blocks can be used for multiplier, counters, filters, and other common functions.

Figure 11: **DSP48 Power Tab**

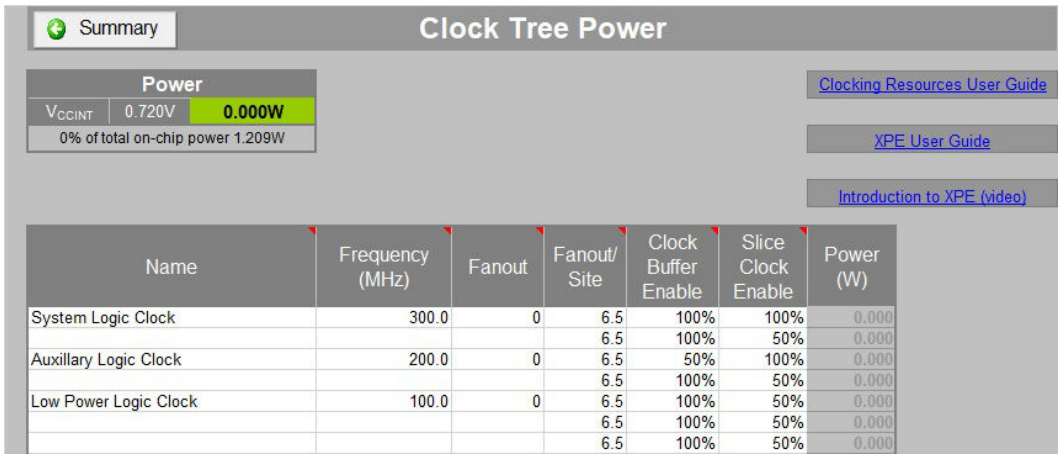


TIP: *The default DSP configuration is assumed to be 27x18 in XPE. The toggle rate must be scaled accordingly for accurate power estimation. For example, if a 18x18 DSP is expected to toggle 25%, then scale it by 0.8 (20%), and enter it into XPE. Similarly, scale the actual toggle rate by 0.53 for a 12x12 configuration. The 0.8 scaling factor is obtained as follows: 1 – ((27 + 18) – (18 + 18))/(27 + 18) = 1 – 9/45 = 0.8.*

Clock Manager Power

If an MMCM/PLL is used in the design, enter the corresponding use and configuration of each. During the early stages of the design, the complete clocking details might not be known. Enter what is known to estimate the power and revisit as the design progresses.

Figure 12: **Clock Manager Power Tab**

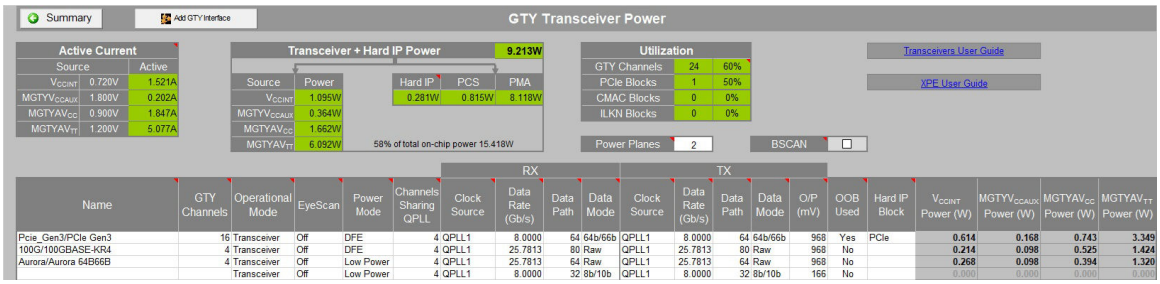


Transceiver Power

Depending on the device selected, the transceiver can be a GTH, GTY, GTM. The best way to fill in the sheet is to use the **Add GTx Interface** button (where x=H, Y, or M).

XPE calculates power for each channel including the power of all associated circuits, shared resources between channels, I/O buffers, reference clock circuitry, and so forth. Therefore, the use of these resources should not be entered on any other sheet (for example, clock or I/O) to describe the transceiver resources.

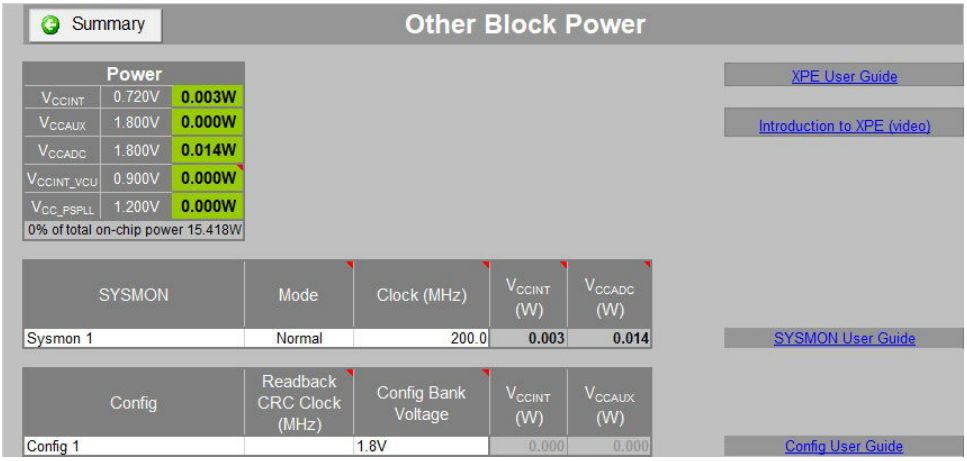
Figure 13: **GTY Transceiver Power Tab**



Other Block Power

Complete this sheet with the details and information on the SYSMON and configuration blocks.

Figure 14: **Other Block Power Tab**



TIP: *Xilinx only supports thermal measurements using SYSMON. Because it is integrated into the silicon, it gives the most accurate measurement possible (±3°C). SYSMON is recommended to be utilized for all designs to monitor T_J and ensure the device junction temperature does not exceed the specification including the error. For example, if 100°C is the maximum T_J of the device, the maximum T_J measured using SYSMON should not be more than 97°C (100°C – 3°C). The SYSMON error value can be found in device data sheets.*

Step 6: Set the Toggle and Connectivity Parameters

For each tab in XPE containing a Toggle Rate, Average Fanout, or Enable Rate, review the set value. For clock fanout, it is crucial that the fanout is entered correctly because it could dramatically impact the clock power. The clock fanout should be the sum of all the entries that are clocked by each clock in the other tabs.

TIP: *To ensure the clock fanout is entered correctly, create an equation that sums all of the synchronous elements for any particular clock domain. For instance, in the Fanout field for a given clock, type =SUM (and then select all of the cells that specify the number of synchronous elements sourced by that clock (that is shift registers, distributed RAMs, block RAMs, DSPs, etc.) and close the parenthesis). The* ***Fanout*** *cell is then populated with the appropriate number. The resulting Excel equation would be similar to this:*

=SUM(LOGIC!G12:I12,BRAM!E10,DSP!E8)

=SUM(IO!I19:K19)

This method of entering clock fanout has the added advantage of automatically updating when adjustments are made to the spreadsheet resource counts.

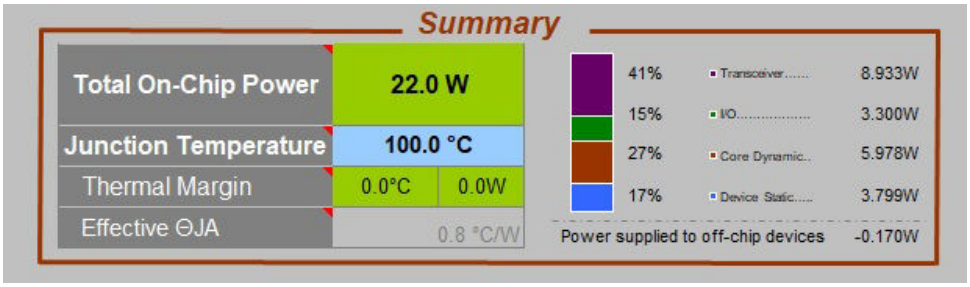
For toggle and enable rates, in the absence of any other information or knowledge, leave these settings at their defaults. However, if you determine that the default might not represent the characteristics of your design, make the necessary adjustments. For instance, if you know that a memory interface has a training pattern routine that exercises a sustained high-toggle rate on that interface, the **Toggle Rate** might need to be raised to reflect this additional activity. Alternatively, if a portion of a circuit is clock enabled in a way that reduces the overall activity of the circuit, the toggle rate might need to be reduced. More information on methods to determine toggle rate are found in *Xilinx Power Estimator User Guide* (UG440).

For I/O Output Load, enter a capacitive load for each design output. It affects the dynamic power of the driven output. The Output Load value is primarily made from the sum of the individual input capacitance of each device connected to that output. The input capacitance is described in the device data sheets.

Step 7: Analyze the Results and Constrain the Design

Update Steps 1 through 6, if necessary, and after completing these steps, analyze the results.

Figure 15: **Summary Panel**



1. The Total On-Chip Power reported is the maximum power for the design and should not exceed the power budget. Analyze if this power is within the desired power and thermal budget for the project. If higher than the budget, adjustments should be made to the resource and power characteristics of the design until an acceptable result is reached.
2. Analyze the various trade-offs to derive the desired functionality with a tighter power budget. The best time to explore these options is early in the design process. After all the data is entered and the design is operating within the thermal limits of the selected device temperature grade, use the power reported by XPE to specify the rails and thermal design adjustments. Depending upon your confidence in the data entered, additional margin of values can help circumvent the possibility of under designing the system for the device selected.
3. Use the Total On-Chip Power value in thermal simulations to model the entire system including the device heat sink, board, other heat sources, case closure, and airflow patterns. Various uncertainties including the thermal model, SYSMON error, power estimation, heat sink, fan, TIM, and PCB irregularities need to be accounted for to build margin in the simulations and to calculate the maximum T_J. To provide a more accurate environment setting, derive an effective θ_{JA} and local ambient values to feed back into the XPE spreadsheet. Ensure that the maximum T_J is not exceeded. Periodically update XPE while the design matures to check that the power and thermal margins are still adequate.

   There are three factors that describe the thermal design:

   - T_J: Junction temperature.
   - T_A: Ambient temperature.
   - P_D: Power dissipation.

   This is shown in the following equation:

   $$\theta_{JA} = (T_J - T_A) / P_D$$

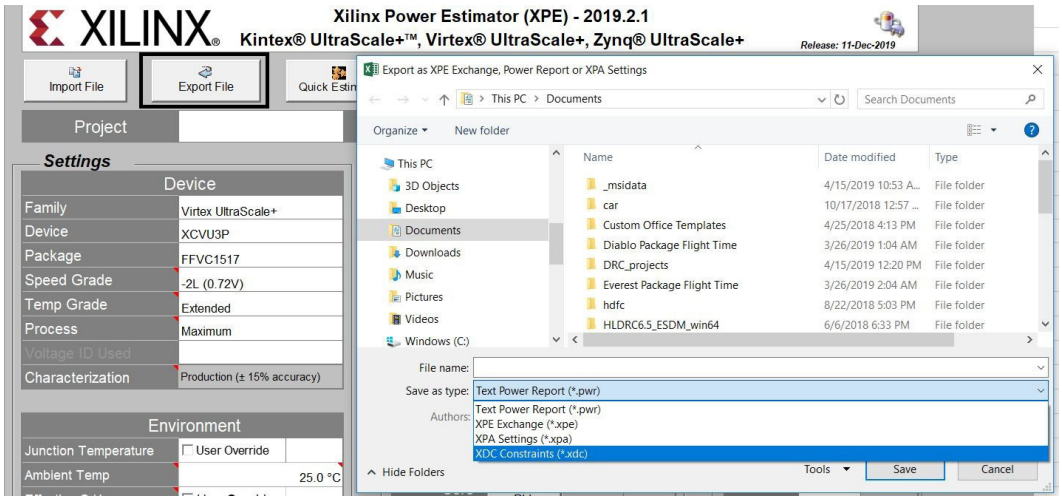
   θ_{JA} represents this relationship in a Celsius per watt (C/W) value. For every watt dissipated, the junction temperature increases by a known value. This value can be reduced by improving the effectiveness of the thermal solution. For designs that exceed junction temperature, and changes to the thermal solution are not possible, one of these attributes *must* be changed:

   - T_J: If possible select a high temperature grade or utilize the excursion to 110°C. For more information, see *Extending the Thermal Solution by Utilizing Excursion Temperatures* (WP517).

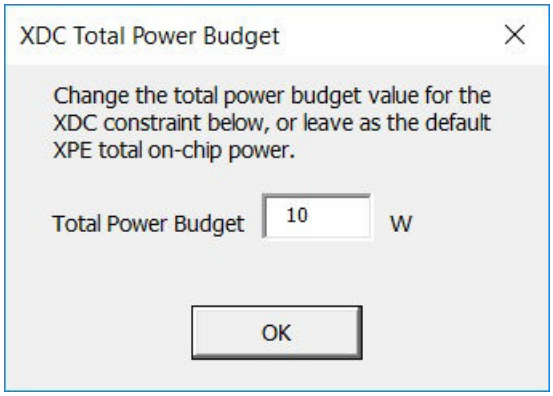
- T_A: Can the ambient temperature of the product be reduced?
- P_D: Reduce the power of the design. Reduce toggling, investigate clock gating, or move to a low-voltage part which can reduce power by up to 30%.

For devices available in lidless packages, this can reduce the θ_{JA} because there is a lower thermal resistance to the user solution. This should be investigated, where possible.

4. After the power budget is defined, constrain the Vivado development using the power Xilinx design constraints (XDC). The XDC constraints are generated by selecting the XDC Constraints file type. In the dialog box, select **XDC Constraints** and specify a file name. Add the constraints to the XDC file of the project to allow the report_power command to analyze the design and report the margin based on the power budget defined at the estimation stage. The goal is to keep the power in compliance even when the application is run on hardware, reducing any added cost or delay to the product.



5. The final step is to add the total power (W) required in the Total Power Budget dialog.



Conclusion

Accurate power estimations are made using the Xilinx Power Estimator tool when accurate data is entered. During the early stages of system design, determining the exact power requirement can be a challenge. However, with the seven steps discussed in this application note, the issues are broken down into smaller, easier to define and understand phases that allow for improved data entry and improved data accuracy. After a power estimation has being finalized, it will directly impact all aspects of the product design, such as power delivery, board, thermal solution, and potentially mechanics. Ensuring that the original power estimation is adhered to is critical for a successful and fast time to market. Any deviation from the power estimation should be acted on as early as possible to reduce impact on the design cycle.

References

These documents provide supplemental material useful with this guide:

1. UltraScale™ and UltraScale+™ device data sheets:
   - *Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS892)
   - *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS893)
   - *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS922)
   - *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923)
   - *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925)
   - *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
11/16/2020 Version 1.0	
Initial release.	N/A

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