

高精度定时器的同步功能

关键字：高精度定时器， 同步

1. 引言

STM32G474 所含的高精度定时器(HRTIMER)其实包含了多个定时器，多个定时器之间可以单独工作，也可以进行同步，且高精度定时器还能与片上的其他定时器以及其他芯片进行同步，本文将对高精度定时器的同步功能进行介绍。

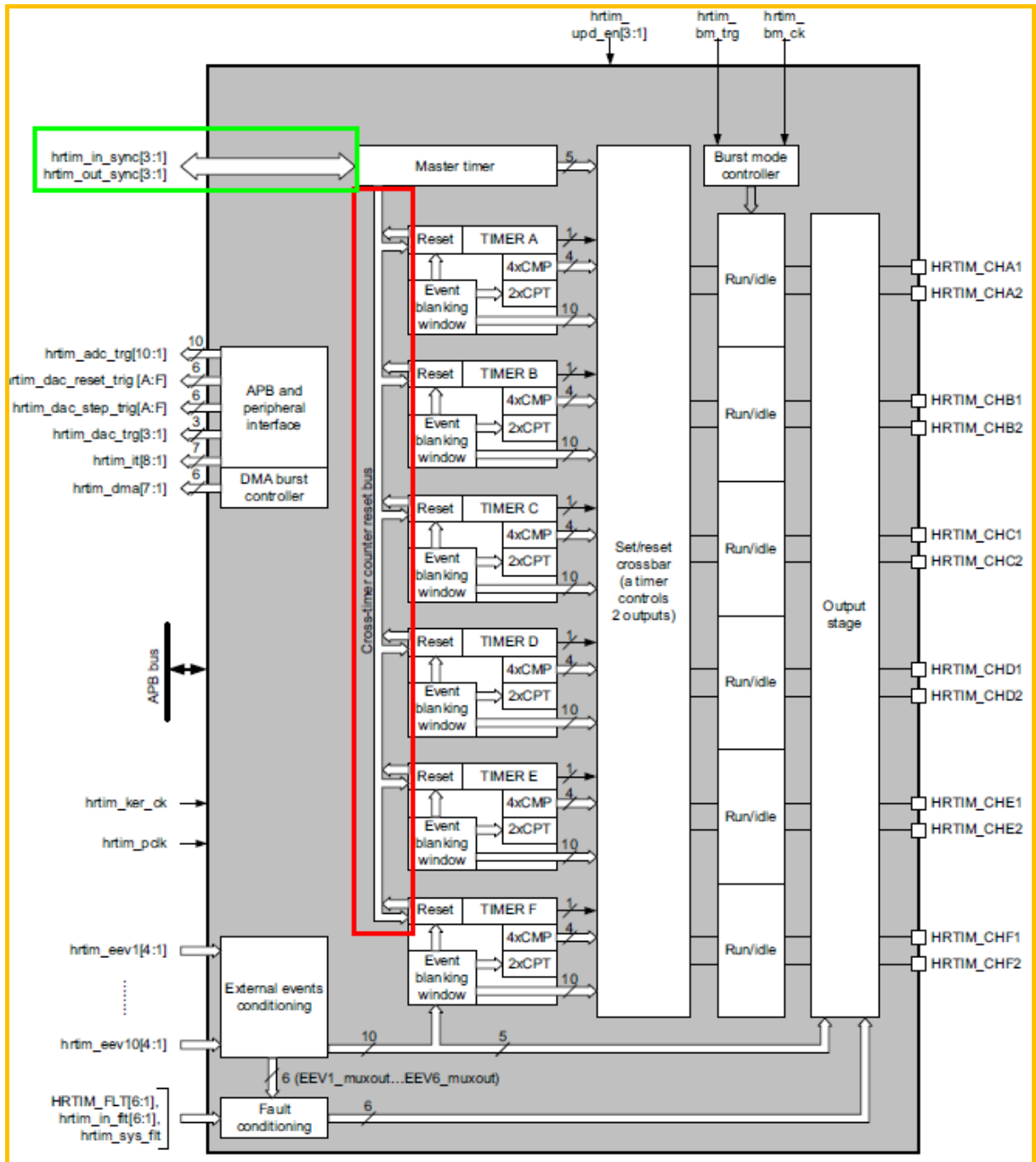
2. 定时器同步结构

HRTIME 的整体架构如下图所示，内含由 7 个定时器，主定时器 Master timer 与子定时器 Timer A~F，为 1 主 6 从结构，同步功能主要分为两部分：

- 内部同步：各定时器通过内部的 Cross-timer counter reset bus 互连，见图中红框标识部分；
- 外部同步：主定时器通过 External Synchronization input/output 单元与片上其他定时器以及片外其他 MCU 的定时器进行同步，如图中绿框标识部分。

整个同步功能的主体是主定时器，其主要作用就是用来给所有子定时器提供统一的同步事件，以及将同步事件提供给外部或是接收外部输入的同步事件。另外子定时器也可将自身的某些事件作为同步事件发送到 Cross-timer counter reset bus 上。

在同步功能中，将提供同步信号的定时器称为主，接收同步信号的称为从。在接收到同步信号后，从定时器将自身的计数器复位到 0 或是启动计数，从而与主定时器实现同步或形成一定的移相。



3. 高精度定时器内部同步

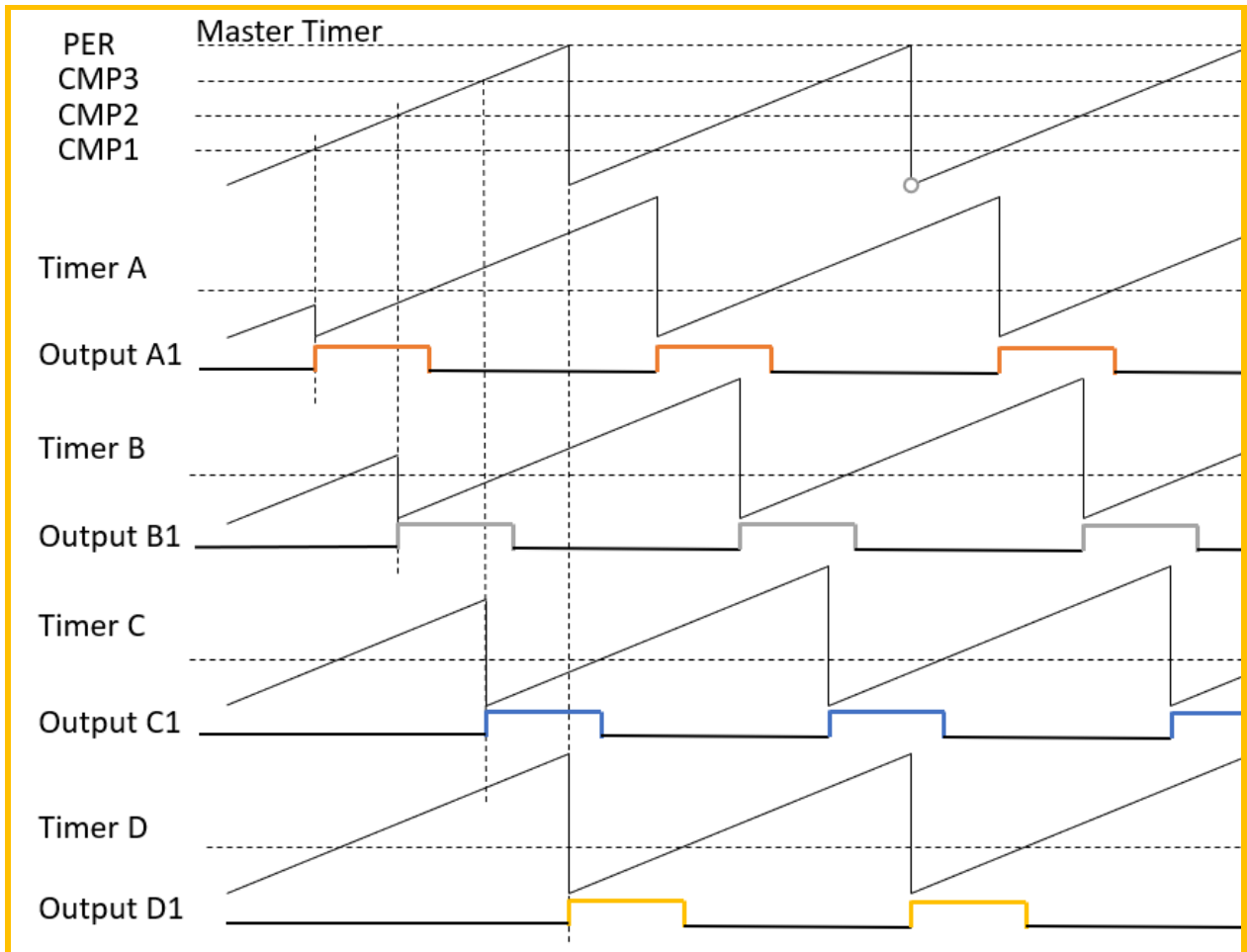
通过内部的互联总线 Cross-timer counter reset bus, **除主定时器 Master Timer 外**,每个定时器都可以接收总线上其他定时器发出的同步信号,同时所有定时器都可将自身的某些事件作为同步信号发送到总线上。以定时器 Timer A 为例,其可以接收到来自 Cross-timer counter reset bus 的同步事件包括:

- Master timer period event

- Master timer cmp1/2/3/4 event
- Timer B cmp1/2/4 event
- Timer C cmp1/2/4 event
- Timer D cmp1/2/4 event
- Timer E cmp1/2/4 event
- Timer F cmp1/2 event

通过 Cross-timer counter reset bus，可以将所有的子定时器都与主定时器进行同步，也可以将所有的定时器分为几组，分别工作。

下面以子定时器都与主定时器同步为例进行说明，借助 CubeMx 配置工具，轻松完成如下图所示的四相 90° 交错 PWM 的产生。



Master Timer 的 PER/CMP1/CMP2/CMP3 事件分别作为 Timer A/B/C/D 的同步源，复位对应的定时器计数器。在子定时器中，分别选择对应的来自 Master Timer 的事件作为自身的同步源。

在 CubeMx 中的相关配置如下的截图(截图仅示意同步功能部分的配置)。

Master Timer 中的配置：

Timer Idx	Master Timer
<ul style="list-style-type: none"> Time Base Setting <ul style="list-style-type: none"> Prescaler Ratio: HRTIM Clock Multiplied by 32 (HRTIM Clock is set in Clock...) fHRCK Equivalent Frequency: 5.44E9 Hz Period: Timer_PER Resulting PWM Frequency: Timer_PER Hz Repetition Counter: 0x00 Mode: The timer operates in continuous (free-running) mode Timing Unit <ul style="list-style-type: none"> Interleaved Mode: Disabled Start On Sync: Synchronization input event has no effect on the timer Reset On Sync: Synchronization input event has no effect on the timer Dac Synchro: No DAC synchronization event generated Preload Enable: Preload enabled: the write access is done into the preload r... Update Gating: Update done independently from the DMA burst transfer co... Repetition Update: Update on repetition enabled Burst Mode: Timer counter clock is maintained and the timer operates n... Interrupt Requests Sources Selection : Please e... 0 Number of Master Timer Internal DMA Request S... 0 Compare Unit 1 <ul style="list-style-type: none"> Compare Unit 1 Configuration: Enable Compare Value: Timer_PER>>2 Compare Unit 2 <ul style="list-style-type: none"> Compare Unit 2 Configuration: Enable Compare Value: Timer_PER>>1 Compare Unit 3 <ul style="list-style-type: none"> Compare Unit 3 Configuration: Enable Compare Value: (Timer_PER*3)>>2 	

更加简单的方式是在使能 CMP1/2/3 后，直接选择 interleaved Mode 的 Quad 选项，这样 CMP1/2/3 就会自动等于 PER/4, (PER*2)/4, (PER*3)/4, 后续即使 Timer_PER 的值更新，CMP1/2/3 也会按照该规则自动更新，无需软件参与。

Timer Idx	Master Timer
<ul style="list-style-type: none"> Time Base Setting <ul style="list-style-type: none"> Prescaler Ratio: HRTIM Clock Multiplied by 32 (HRTIM Clock is set in Clock...) fHRCK Equivalent Frequency: 5.44E9 Hz Period: Timer_PER Resulting PWM Frequency: Timer_PER Hz Repetition Counter: 0x00 Mode: The timer operates in continuous (free-running) mode Timing Unit <ul style="list-style-type: none"> Interleaved Mode: Quad :CMP1 value is set to the quarter of the Timer Period;... Start On Sync: Synchronization input event has no effect on the timer Reset On Sync: Synchronization input event has no effect on the timer Dac Synchro: No DAC synchronization event generated Preload Enable: Preload enabled: the write access is done into the preload r... Update Gating: Update done independently from the DMA burst transfer co... Repetition Update: Update on repetition enabled Burst Mode: Timer counter clock is maintained and the timer operates n... * Interrupt Requests Sources Selection : Please en... 0 Number of Master Timer Internal DMA Request S... 0 Compare Unit 1 <ul style="list-style-type: none"> Compare Unit 1 Configuration: Enable Compare Unit 2 <ul style="list-style-type: none"> Compare Unit 2 Configuration: Enable Compare Unit 3 <ul style="list-style-type: none"> Compare Unit 3 Configuration: Enable Compare Unit 4 <ul style="list-style-type: none"> Compare Unit 4 Configuration: Disable 	

Timer A 中的配置:

Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please enter the num...	0
Reset Update	Update by Timer reset / roll-over enabled
Resynchronized Update	Update taken into account immediately
Reset Trigger Sources Selection : Please enter the numb...	1
1st Reset Trigger Source	The timer counter is reset upon master timer period event
Interrupt Requests Sources Selection : Please enter the ...	0
Number of Timer A Internal DMA Request Sources - you ...	0

✓ Output 1 Configuration	
Output1 Configuration	TA1
Polarity	Output is active HIGH
Set Source Selection : Please enter the number of Active Set Sources	1
1st Set Source	The master timer period event forces the output to its active state
Reset Source Selection : Please enter the number of Active Reset Sources	1
1st Reset Source	Timer compare 1 event forces the output to its inactive state

Timer B 中的配置:

Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please enter the num...	0
Reset Update	Update by Timer reset / roll-over enabled
Resynchronized Update	Update taken into account immediately
Reset Trigger Sources Selection : Please enter the numb...	1
1st Reset Trigger Source	The timer counter is reset upon master timer Compare 1 event
Interrupt Requests Sources Selection : Please enter the ...	0
Number of Timer A Internal DMA Request Sources - you ...	0

✓ Output 1 Configuration	
Output1 Configuration	TB1
Polarity	Output is active HIGH
Set Source Selection : Please enter the number of Active Set Sources	1
1st Set Source	Master Timer compare 1 event forces the output to its active state
Reset Source Selection : Please enter the number of Active Reset Sources	1
1st Reset Source	Timer compare 1 event forces the output to its inactive state

Timer C 中的配置:

Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please enter the num...	0
Reset Update	Update by Timer reset / roll-over enabled
Resynchronized Update	Update taken into account immediately
Reset Trigger Sources Selection : Please enter the numb...	1
1st Reset Trigger Source	The timer counter is reset upon master timer Compare 2 event
Interrupt Requests Sources Selection : Please enter the ...	0
Number of Timer A Internal DMA Request Sources - you ...	0

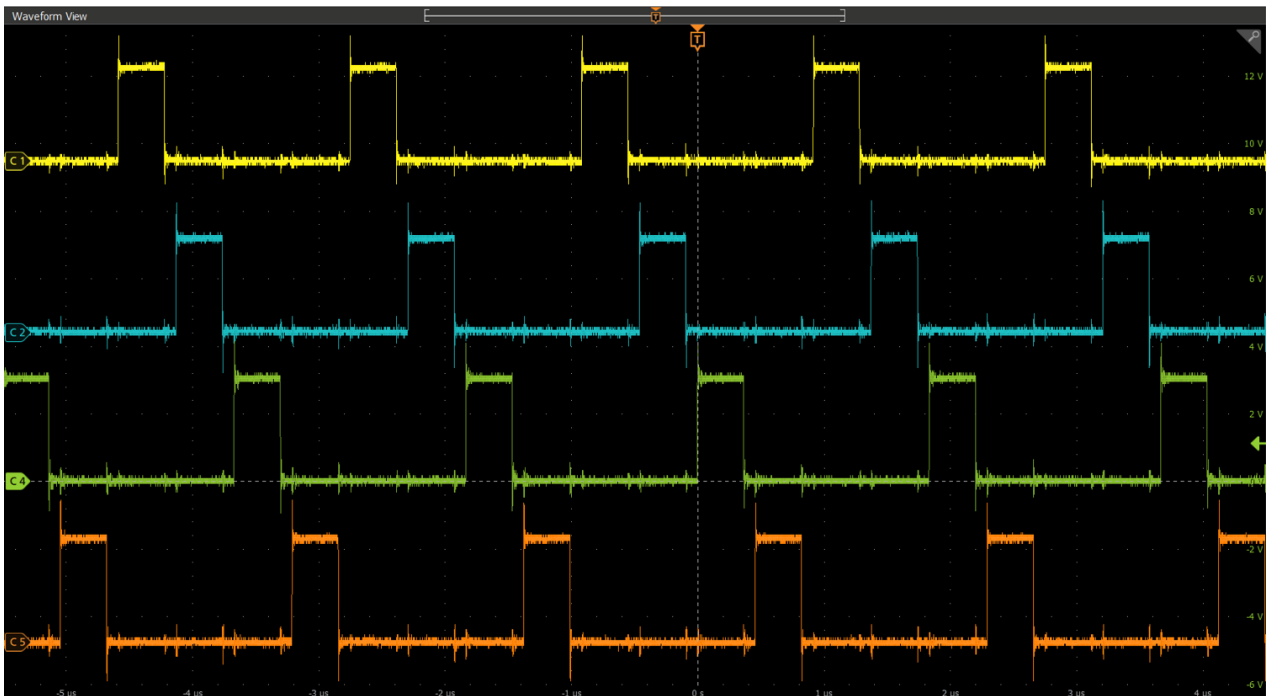
✓ Output 1 Configuration	
Output1 Configuration	TC1
Polarity	Output is active HIGH
Set Source Selection : Please enter the number of Active Set Sources	1
1st Set Source	Master Timer compare 2 event forces the output to its active state
Reset Source Selection : Please enter the number of Active Reset Sources	1
1st Reset Source	Timer compare 1 event forces the output to its inactive state

Timer D 中的配置:

Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please enter the num...	0
Reset Update	Update by Timer reset / roll-over enabled
Resynchronized Update	Update taken into account immediately
Reset Trigger Sources Selection : Please enter the numb...	1
1st Reset Trigger Source	The timer counter is reset upon master timer Compare 3 event
Interrupt Requests Sources Selection : Please enter the ...	0
Number of Timer A Internal DMA Request Sources - you ...	0

Output 1 Configuration	
Output1 Configuration	TD1
Polarity	Output is active HIGH
Set Source Selection : Please enter the number of Active Set Sources	1
1st Set Source	Master Timer compare 3 event forces the output to its active state
Reset Source Selection : Please enter the number of Active Reset Sources	1
1st Reset Source	Timer compare 1 event forces the output to its inactive state

按照以上的同步配置，并设置 PWM 的 Duty = 20%，实测到的四相 90° 交错 PWM 波形如下所示。



4. 高精度定时器外部同步

HRTIME 通过其 Master Timer 的 External Synchronization input/output 单元与片上其他定时器以及片外其他 MCU 的定时器进行同步。

当 HRTIME 做为主时，其输出的同步事件可由其内部的以下事情产生：

- Master Timer start event
- Master Timer CMP1 event
- Timer A start event
- Timer A CMP1 event

该同步事件可以在管脚 HRTIM_SCOUT 上输出一个高或是低的脉冲，宽度为 16 个 f_{hrtim} 周期，同时也可以映射到内部的 ITR10，ITR10 可以直接作为片上其他定时器的同步事件。

Table 250. TIMx internal trigger connection

TIMx	TIM1	TIM8	TIM20
tim_itr0	Reserved	tim1_trgo	tim1_trgo
tim_itr1	tim2_trgo	tim2_trgo	tim2_trgo
tim_itr2	tim3_trgo	tim3_trgo	tim3_trgo
tim_itr3	tim4_trgo	tim4_trgo	tim4_trgo
tim_itr4	tim5_trgo	tim5_trgo	tim5_trgo
tim_itr5	tim8_trgo	Reserved	tim8_trgo
tim_itr6	tim15_trgo	tim15_trgo	tim15_trgo
tim_itr7	tim16_oc1	tim16_oc1	tim16_oc1
tim_itr8	tim17_oc1	tim17_oc1	tim17_oc1
tim_itr9	tim20_trgo	tim20_trgo	Reserved
tim_itr10	hrtim_out_sync2	hrtim_out_sync2	hrtim_out_sync2
tim_itr11..15	Reserved		

当 HRTIME 做为从时，其接收的同步事件可以来自于：

- 片上定时器 TIM1 的 TRGO
- 同步输入管脚 HRTIM_SCIN 的上升沿

接收到同步信号后，可以设置 HRTIME 内部定时器是复位还是启动。

下面以 HRTIME 做为主，TIM1 作为从，HRTIME 的 Timer A 产生一路 PWM，TIM1 产生一路 PWM，两路 PWM 构成两相 180° 交错来说明 HRTIME 的外部同步功能。在 CubeMx 中的关键配置如下截图所示(截图仅示意同步功能的配置)。

HRTIME 配置，HRTIME 作为主，Master timer 的 CMP1 事件做为同步事件，且同步事件映射到内部的 ITR10(也可以将同步信号输出到 HRTIM_SCOUT，同时将信号连接到 TIM1 的 ETR 管脚，由于要多占用两个管脚，不建议该方式)。

同步配置：

Master Timer 配置(可以修改 CMP1 的值来形成不同的移相值)：

Timer Idx	Master Timer
<ul style="list-style-type: none"> Time Base Setting <ul style="list-style-type: none"> Prescaler Ratio: HRTIM Clock (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz) 1.7E8 Hz Period: Timer_PER Resulting PWM Frequency: Timer_PER Hz Repetition Counter: 0x00 Mode: The timer operates in continuous (free-running) mode Timing Unit <ul style="list-style-type: none"> Interleaved Mode: Disabled Start On Sync: Synchronization input event has no effect on the timer Reset On Sync: Synchronization input event has no effect on the timer Dac Synchro: No DAC synchronization event generated Preload Enable: Preload enabled: the write access is done into the preload register Update Gating: Update done independently from the DMA burst transfer completion Repetition Update: Update on repetition enabled Burst Mode: Timer counter clock is maintained and the timer operates normally * Interrupt Requests Sources Selection : Please enter the number of Active Interrupt R... 0 Number of Master Timer Internal DMA Request Sources - you first have to enable th... 0 	
<ul style="list-style-type: none"> Compare Unit 1 <ul style="list-style-type: none"> Compare Unit 1 Configuration: Enable Compare Value: Timer_PER>>1 	

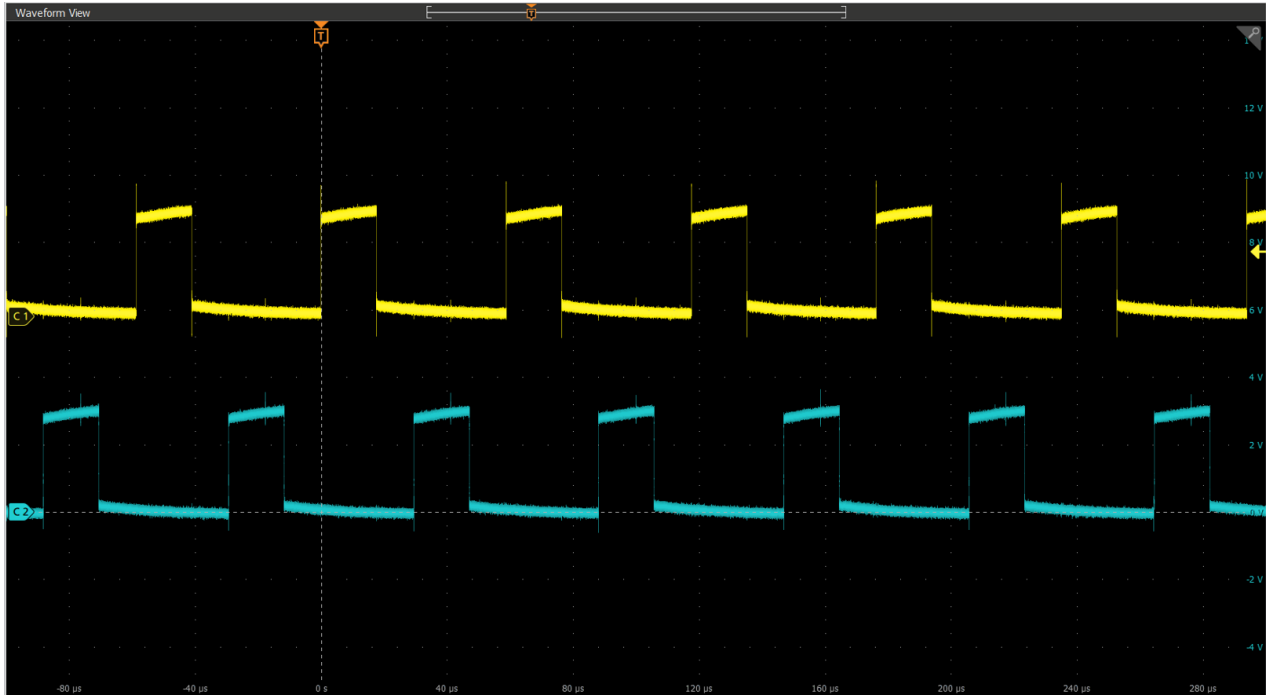
Timer A 配置:

Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please enter the num...	0
Reset Update	Update by Timer reset / roll-over enabled
Resynchronized Update	Update taken into account immediately
Reset Trigger Sources Selection : Please enter the numb...	1
1st Reset Trigger Source	The timer counter is reset upon master timer period event
Interrupt Requests Sources Selection : Please enter the ...	0
Number of Timer A Internal DMA Request Sources - you ...	0

TIM1 的配置，TIM1 做从，工作在 Reset Mode，PWM 的输出模式为 PWM_MODE1。

TIM1 Mode and Configuration	
Mode	
Slave Mode	Reset Mode
Trigger Source	TR10
Clock Source	Internal Clock
Channel1	PWM Generation CH1 CH1N
Channel2	Disable
Configuration	
Reset Configuration	
<ul style="list-style-type: none"> Parameter Settings User Constants NVIC Settings DMA Settings GPIO Settings 	
Configure the below parameters :	
<input type="text" value="Search (Ctrl+F)"/>	
<ul style="list-style-type: none"> Counter Settings <ul style="list-style-type: none"> Prescaler (PSC - 16 bits value): 0 Counter Mode: Up Dithering: Disable Counter Period (AutoReload Register - 16 bits value): Timer_PER Internal Clock Division (CKD): No Division Repetition Counter (RCR - 16 bits value): 0 auto-reload preload: Enable Slave Mode Controller: Reset Mode > Trigger Output (TRGO) Parameters > Break And Dead Time management - BRK Configuration > Break And Dead Time management - BRK2 Configuration > Break And Dead Time management - Output Configuration > Clear Input PWM Generation Channel 1 and 1N <ul style="list-style-type: none"> Mode: PWM mode 1 Pulse (16 bits value): Pulse_Width Output compare preload: Enable Fast Mode: Disable CH Polarity: High CH1N Polarity: High CH Idle State: Reset 	

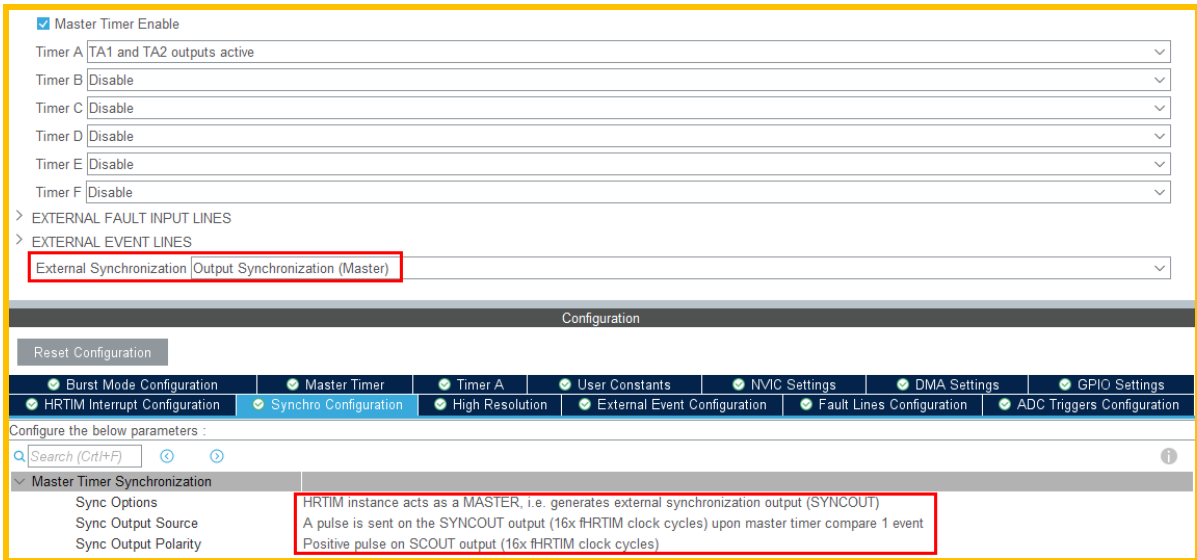
按照以上的同步配置，实测到的两 180° 交错 PWM 波形如下所示。



C1: HRTIM_TA1 C2 : TIM1_CH1

接下来再以如何在两个 MCU 的 HRTIME 之间完成同步。比如 MCU1 的 HRTIME 做主设备，MCU2 的 HRTIME 做从设备，相关的配置如下截图所示。

MCU1 的 HRTIME 同步配置，Master timer 的 CMP1 事件做为同步事件，同步信号必须输出到 HRTIM_SCOUT 管脚上。



MCU1 Master Timer 配置(可以修改 CMP1 的值来形成不同的移相值):

Timer Idx	Master Timer
Time Base Setting	
Prescaler Ratio	HRTIM Clock (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz)
fHRCK Equivalent Frequency	1.7E8 Hz
Period	Timer_PER
Resulting PWM Frequency	Timer_PER Hz
Repetition Counter	0x00
Mode	The timer operates in continuous (free-running) mode
Timing Unit	
Interleaved Mode	Disabled
Start On Sync	Synchronization input event has no effect on the timer
Reset On Sync	Synchronization input event has no effect on the timer
Dac Synchro	No DAC synchronization event generated
Preload Enable	Preload enabled: the write access is done into the preload register
Update Gating	Update done independently from the DMA burst transfer completion
Repetition Update	Update on repetition enabled
Burst Mode	Timer counter clock is maintained and the timer operates normally
* Interrupt Requests Sources Selection : Please enter the number of Active Interrupt R...	0
Number of Master Timer Internal DMA Request Sources - you first have to enable th...	0
Compare Unit 1	
Compare Unit 1 Configuration	Enable
Compare Value	Timer_PER>>1

MCU1 Timer A 配置:

Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please enter the num...	0
Reset Update	Update by Timer reset / roll-over enabled
Resynchronized Update	Update taken into account immediately
Reset Trigger Sources Selection : Please enter the numb...	1
1st Reset Trigger Source	The timer counter is reset upon master timer period event
Interrupt Requests Sources Selection : Please enter the ...	0
Number of Timer A Internal DMA Request Sources - you ...	0

同时需要在程序中添加如下的 PB1 初始化代码，保证同步脉冲能在 PB1 上产生。

```

/* USER CODE BEGIN HRTIM1_MspPostInit 1 */
GPIO_InitStruct.Pin = GPIO_PIN_1;
GPIO_InitStruct.Mode = GPIO_MODE_AF_PP;
GPIO_InitStruct.Pull = GPIO_NOPULL;
GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_VERY_HIGH;
GPIO_InitStruct.Alternate = GPIO_AF13_HRTIM1;
HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);
/* USER CODE END HRTIM1_MspPostInit 1 */
    
```

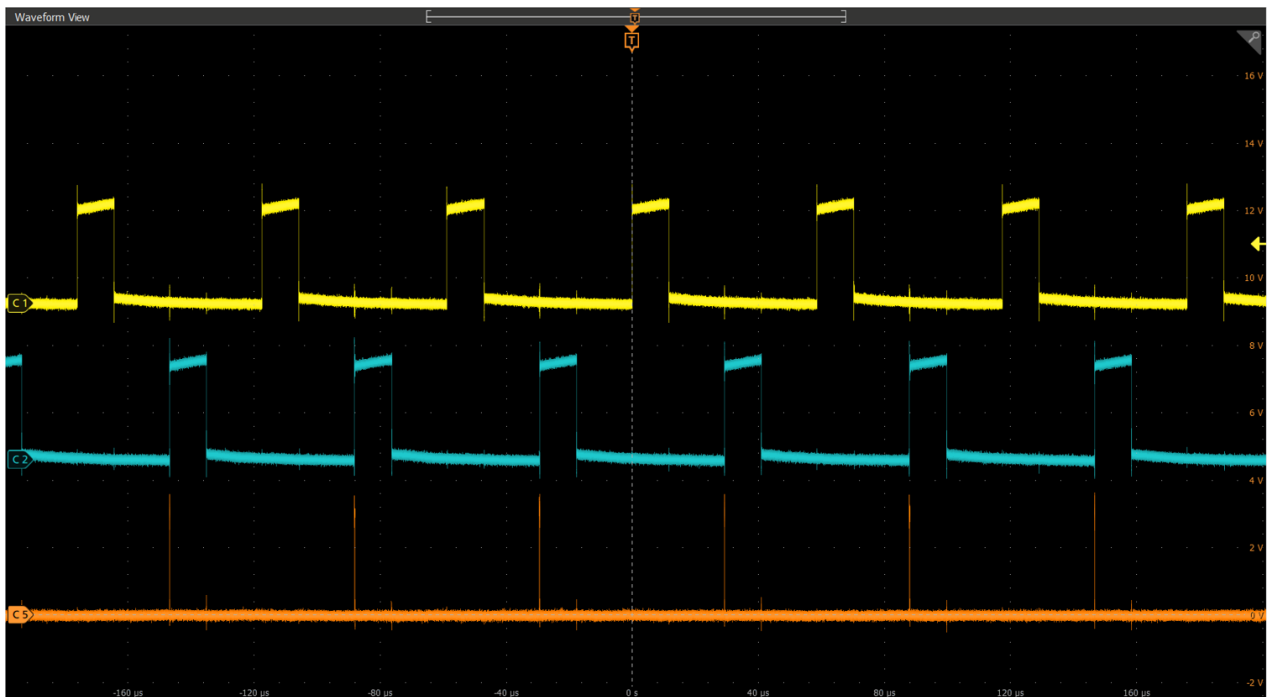
MCU2 的 HRTIME 同步配置，同步信号来自 HRTIM_SCIN。

<input checked="" type="checkbox"/> Master Timer Enable	
Timer A [TA1 and TA2 outputs active]	▼
Timer B	Disable ▼
Timer C	Disable ▼
Timer D	Disable ▼
Timer E	Disable ▼
Timer F	Disable ▼
> EXTERNAL FAULT INPUT LINES	
> EXTERNAL EVENT LINES	
External Synchronization	Input Synchronization (Slave) ▼
Configuration	
Reset Configuration	
<input checked="" type="checkbox"/> Burst Mode Configuration	<input checked="" type="checkbox"/> Master Timer
<input checked="" type="checkbox"/> HRTIM Interrupt Configuration	<input checked="" type="checkbox"/> Synchro Configuration
<input checked="" type="checkbox"/> High Resolution	<input checked="" type="checkbox"/> External Event Configuration
<input checked="" type="checkbox"/> Fault Lines Configuration	<input checked="" type="checkbox"/> ADC Triggers Configuration
Configure the below parameters :	
Search (Ctrl+F)	①
Master Timer Synchronization	
Sync Options	HRTIM instance acts as a SLAVE, i.e. it is synchronized by external sources (SYNCIN)
Sync Input Source	A positive pulse on SYNCIN input triggers the HRTIM

MCU2 Timer A 的配置，来自 HRTIM_SCIN 的同步信号让 Timer A 复位并启动计数。

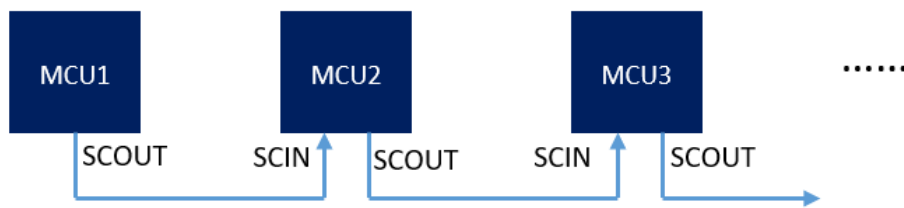
General Timer Idx Basic/Advanced Configuration Time Base Setting Prescaler Ratio fHCLK Equivalent Frequency Period Resulting PWM Frequency Repetition Counter Up Down Mode Mode Timing Unit Interleaved Mode Start On Sync Reset On Sync Dac Synchro Preload Enable Update Gating Repetition Update	Timer A Advanced (using HAL_Waveform methods) HRTIM Clock (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz) 1.7E8 Hz Timer_PER Timer_PER Hz 0x00 Timer counter is operating in up-counting mode The timer operates in continuous (free-running) mode Disabled Synchronization input event starts the timer Synchronization input event resets the timer No DAC synchronization event generated Preload enabled: the write access is done into the preload register Update done independently from the DMA burst transfer completion Update on repetition disabled
Output 1 Configuration Output1 Configuration Polarity Set Source Selection : Please enter the number of Active Set Sources 1st Set Source Reset Source Selection : Please enter the number of Active Reset Sources 1st Reset Source	TA1 Output is active HIGH 1 Timer counter reset event coming solely from software or SYNC input forces the output to its active state 1 Timer compare 1 event forces the output to its inactive state

按照以上的同步配置，并设置 MCU1 与 MCU2 的 Timer A 的 PWM 的 Duty = 20%，实测到的两 180° 交错 PWM 波形如下所示。



C1 : MCU1 TA1 C2 : MCU2 TA1 C5 : HRTIM 同步脉冲

通过 HRTIM_SCIN 与 HRTIM_SCOUT，配合 HRTIME 同时做主与从的方式，可以实现多个 MCU 之间定时器的同步，如下图示意。



5. 小结

对高精度定时器 HRTIME 的同步功能进行了介绍，基于 STM32G474 和 CubeMx 工具说明如何快速的实现 HRTIME 的各种同步功能。

版本历史

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