

VPK180 Evaluation Board User Guide

UG1582 (v1.0) February 21, 2023

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Introduction

Overview

The VPK180 evaluation board features the Xilinx® Versal® ACAP XCVP1802 device. The VPK180 board enables the demonstration, evaluation, and development of the applications listed here, as well as other customer applications. Many features found on the VPK180 board are subsets of existing Versal ACAP boards (e.g., the VCK190 and VMK180 boards).

- Fiber optic
- Communications
- Data center compute acceleration
- Aerospace and defense
- Test and measurement

The VPK180 evaluation board is equipped with many of the common board-level features needed for design development, including:

- OSFP optical transceiver support
- QSFP-DD optical transceiver support
- SFP-DD optical transceiver support
- LPDDR4 component memory
- USB
- Ethernet networking interface
- One FMC+ expansion port

Models of Boards

The following table lists the models for the VPK180 evaluation board. See the [VPK180 Evaluation Board](#) product page for details

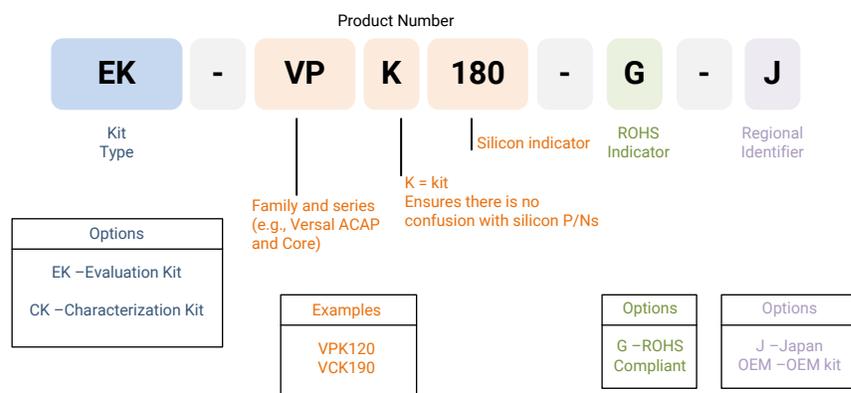
Table 1: Models of VPK180 Evaluation Boards

Kit	Description
EK-VPK180-G	Xilinx Versal ACAP VPK180 evaluation kit
EK-VPK180-G-J	Xilinx Versal ACAP VPK180 evaluation kit, Japan specific

Versal ACAP Kit Numbering

The Versal ACAP kit numbering is illustrated in the following figure.

Figure 1: Kit Numbering



X26520-111822

Navigating Content by Design Process

Xilinx® documentation is organized around a set of standard design processes to help you find relevant content for your current development task. All Versal® ACAP design process [Design Hubs](#) and the [Design Flow Assistant](#) materials can be found on the [Xilinx.com](#) website. This document covers the following design processes:

- **Board System Design:** Designing a PCB through schematics and board layout. Also involves power, thermal, and signal integrity considerations. For more information, see [Versal ACAP Design Process Documentation Board System Design](#).

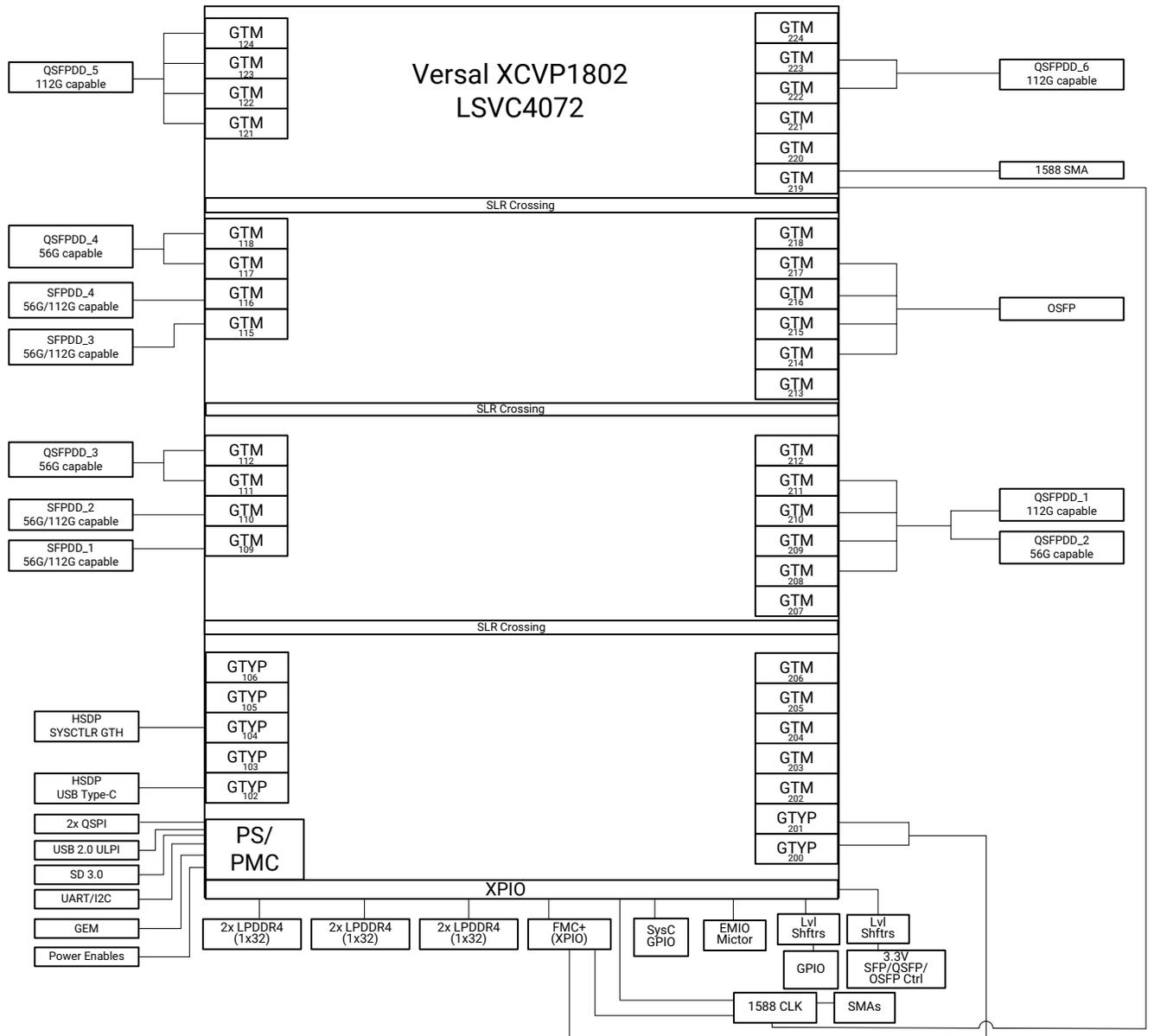
Additional Resources

See [Appendix D: Additional Resources and Legal Notices](#) for references to documents, files, and resources relevant to the VPK180 evaluation board.

Block Diagram

A block diagram of the VPK180 evaluation board is shown in the following figure.

Figure 2: Evaluation Board Block Diagram



X26519-110222

Board Features

The VPK180 evaluation board features are listed here. Detailed information for each feature is provided in [Chapter 3: Board Component Descriptions](#).

- XCVP1802, LSVC4072 package
- Form factor: see [Board Specifications](#)
- Onboard configuration from:
 - USB-to-JTAG bridge
 - JTAG pod 2 mm 2x7 flat cable connector
 - microSD card (PS MIO I/F)
 - Quad SPI (QSPI)/eMMC (system controller I/F)
 - Dual QSPI
- Clocks
 - ACAP bank 702/5/8 Si570 LPDDR4_CLK1/2/3 (DIMM) 200 MHz
 - ACAP bank 503 Si570 REF_CLK 33.3333 MHz
 - ACAP bank 503 RTC Xtal 32.768 kHz
 - IEEE-1588 eCPRI 8A34001 clocks (various)
 - ACAP bank GTY102/4 (REFCLK0) HSDP dedicated clocks
 - ACAP bank GTY200/1 (REFCLK0) FMC provided
 - ACAP banks GTM109, GTM110, GTM111, GTM112, GTM115, GTM116, GTM117, GTM118 RC21008A 156.25 MHz
 - ACAP banks GTM208, GTM209, GTM210, GTM211, GTM214, GTM215, GTM216, GTM217 RC21008A 156.25 MHz
- Three LPDDR4 interfaces (2x32-bit 4 GB components each)
 - XPIO triplet 1 (banks 700, 701, 702)
 - XPIO triplet 2 (banks 703, 704, 705)
 - XPIO triplet 3 (banks 706, 707, 708)
- PL FMCP HSPC (FMC+) connectivity
 - FMCP1 HSPC full LA[00:33] bus

- PL GPIO connections
 - PL UART1 to FTDI
 - PL GPIO DIP switch (4-position)
 - PL GPIO LEDs (four)
 - PL GPIO pushbuttons (two)
 - PL trace connector (J332)
 - PL SYSCTLR_GPIO[0:15]
 - PL 8A34001_GPIO[0:7, 10:15]
- 28 PL GTYP transceivers (7 quads)
 - Not used (18, bank GTYP102, GTYP103, GTYP104, GTYP105, GTYP106)
 - System controller HSDP (1, banks GTYP104)
 - USB-C HSDP (1, banks GTYP102)
 - FMCP1 HSPC DP (8, banks GTYP200, GTYP201)
- 140 PL GTM transceivers (35 quads)
 - Not used (74, bank GTM109, GTM110, GTM115, GTM116, GTM121, GTM122, GTM123, GTM124, GTM202, GTM203, GTM204, GTM205, GTM206, GTM207, GTM212, GTM213, GTM214, GTM215, GTM216, GTM217, GTM218, GTM219, GTM220, GTM221, GTM222, GTM223, GTM224)
 - QSPDD1 (8, banks GTM208, GTM209, GTM210, GTM211)
 - QSPDD2 (8, banks GTM208, GTM209, GTM210, GTM211)
 - Note:* QSPDD1 and QSPDD2 are interleaved.
 - QSPDD3 (8, banks GTM111, GTM112)
 - QSPDD4 (8, banks GTM117, GTM118)
 - QSPDD5 (8, banks GTM121, GTM122, GTM123, GTM124)
 - QSPDD6 (8, banks GTM221, GTM222, GTM223, GTM224)
 - OSFP (8, banks GTM214, GTM215, GTM216, GTM217)
 - SFPDD1 (2, bank GTM109)
 - SFPDD2 (2, bank GTM110)
 - SFPDD3 (2, bank GTM115)
 - SFPDD4 (2, bank GTM116)

- User SMA connectors (1, bank GTM219)
- 8A34001 CLK (1, bank GTM219)
- PS PMC MIO connectivity
 - PS MIO[0:12]: boot configuration QSPI
 - DC QSPI support
 - PS MIO[13:25]: USB2.0
 - PS MIO[26:36, 51]: SD1 I/F
 - PS MIO[37]: ZU4_TRIGGER
 - PS MIO[38]: Not connected
 - PS MIO[39:41]: SYSMON_I2C
 - PS MIO[42:43]: UART0 to FTDI
 - PS MIO[44:47]: I2C1, I2C0
 - PS MIO[48], PS LPD MIO[0:11, 24:25]: GEM0 RGMII Ethernet RJ-45
 - PS MIO[49] and LPD MIO[13,15:16,20]: power enable
 - PS MIO[50] and LPD MIO[18:19]: Not connected
 - PS LPD MIO [21:22]: optional fan interface
 - LPD MIO[23]: VADJ_FMC power rail
- Security: PSBATT button battery backup
- SYSMON header
- Operational switches (power on/off, PROG_B, boot mode DIP switch)
- Operational status LEDs (INIT, DONE, PS STATUS, PGOOD)
 - See [Power and Status LEDs](#)
- Power management
- System controller (XCZU4EG)

The VPK180 evaluation board provides a rapid prototyping platform using the XCVP1802-2MSELSVC4072 device. See the *Versal Architecture and Product Data Sheet: Overview (DS950)* for a feature set overview, description, and ordering information.

Board Specifications

Dimensions

Height: 12.360 inches (31.394 cm)

Length: 11.504 inches (29.22016 cm)

Thickness: 131.5 mil $\pm 10\%$ (3.3401 $\pm 10\%$)

Note: A 3D model of this board is not available.

See the [VPK180 Evaluation Board](#) website for the XDC listing and board schematics.

Environmental

Note: The operating temperature range is not fully tested across the specified temperature range. It is for general guidelines only. Customers should use the VPK180 evaluation board for evaluation purposes only in a normal lab environment and should not operate beyond room temperature.

- **Temperature:**

Operating: 0°C to +45°C

Storage: -25°C to +60°C

- **Humidity:** 5% to 95% non-condensing

Operating Voltage

+12 V_{DC}

Mechanical

The VPK180 evaluation board includes a mechanical stiffener to help ensure success with the board under normal lab conditions and use. While it is recommended to not remove this stiffener, it is understood that it might be necessary to remove it for continued evaluation.

The mechanical stiffener screw torque is 4.5 in-lbs. When attaching or removing the mechanical stiffener, ensure proper ESD precautions are taken. See [Standard ESD Measures](#) for suggestions on best practices.

- Removing the Stiffener

With power and other cabling unplugged, carefully unscrew the eleven 4-40 screws in any order. Care needs to be taken with the cooling solution as the board is manipulated due to potential excessive forces.

- Attaching the Stiffener

With power and other cabling unplugged, carefully align the PCBA standoff holes to the sheet metal tray (stiffener) standoffs. Next, it is suggested to insert two screws in opposite corners of the board/tray combination. Loosely tighten the screws to aid in alignment. Add the remaining seven screws and loosely tighten. Finally, in a left to right or right to left pattern, tighten all nine screws to 4.5 in-lbs.

Note: The tray will only fit one direction with the transceiver connectors having cutouts below. See [Board Component Descriptions](#) for more information.

Board Setup and Configuration

Standard ESD Measures



CAUTION! ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.

To prevent ESD damage:

- Attach a wrist strap to an unpainted metal surface of your hardware to prevent electrostatic discharge from damaging your hardware.
- When you are using a wrist strap, follow all electrical safety procedures. A wrist strap is for static control. It does not increase or decrease your risk of receiving electric shock when you are using or working on electrical equipment.
- If you do not have a wrist strap, before you remove the product from ESD packaging and installing or replacing hardware, touch an unpainted metal surface of the system for a minimum of five seconds.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system.
- With the device still in its antistatic bag, touch it to the metal frame of the system.
- Grasp cards and boards by the edges. Avoid touching the components and gold connectors on the adapter.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before you pick it up again, touch the antistatic bag and the metal frame of the system at the same time.
- Handle the devices carefully to prevent permanent damage.

Board Component Location

The following figure shows the VPK180 board component locations. Each numbered component shown in the figure is keyed to the table in [Board Component Descriptions](#).

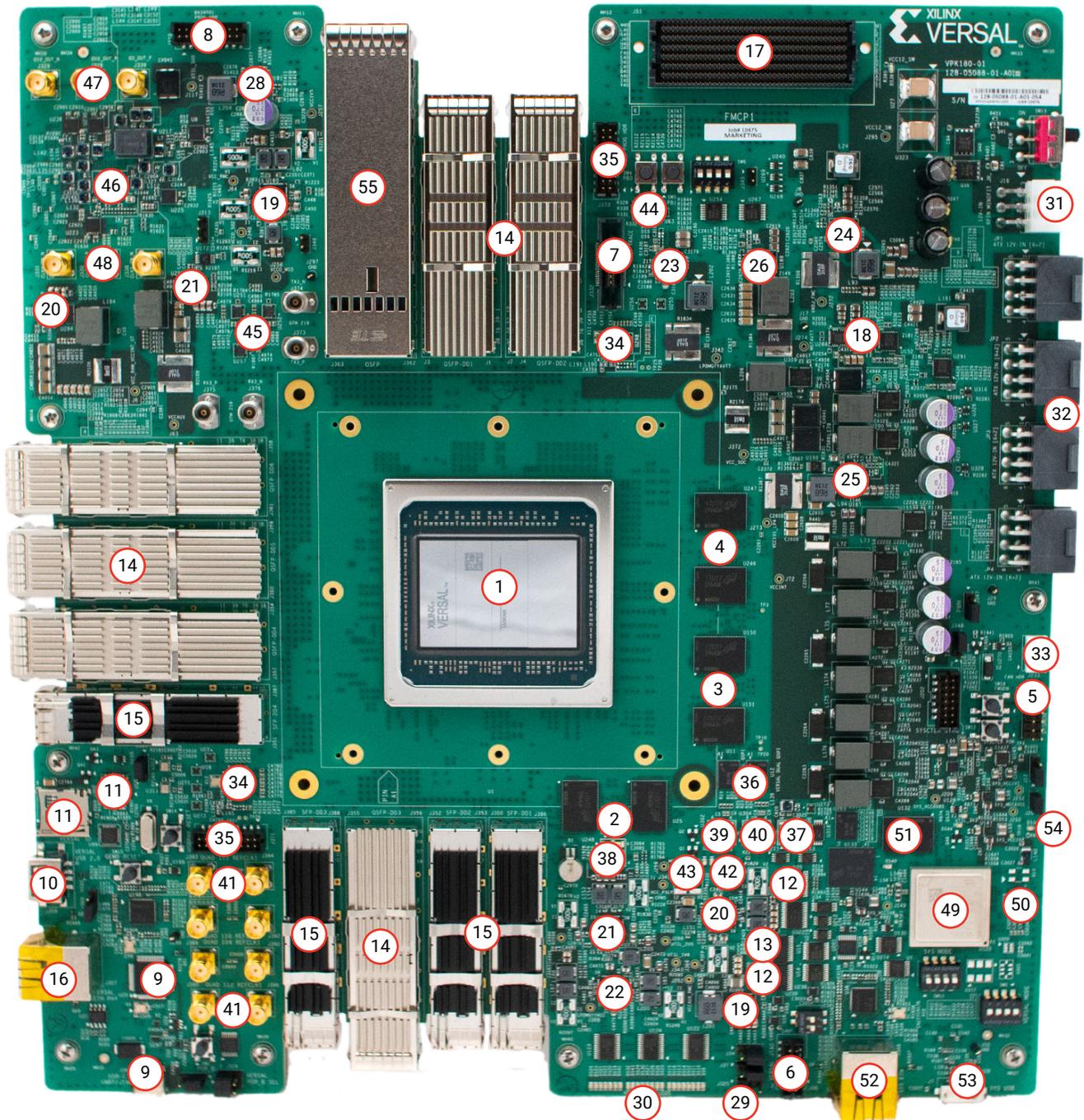
 **IMPORTANT!** *The following figure is for visual reference only and might not reflect the current revision of the board.*

 **IMPORTANT!** *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific VPK180 version of interest for such details.*

Figure 3: Evaluation Board Component Locations

⓪ Round callout references a component on the front side of the board

⓪⓪ Square callout references a component on the back side of the board



X27290-101422

Board Component Descriptions

The following table identifies the components and references the respective schematic (038-05088-01) page numbers.



CAUTION! Do NOT plug a PC ATX power supply 6-pin connector into the VPK180 board power connector J16. The ATX 6-pin connector has a different pinout than J16. Connecting an ATX 6-pin connector into J16 damages the VPK180 board and voids the board warranty.

Table 2: Board Component Locations

Callout No.	Ref. Des.	Feature	Notes	Schematic Page
1	U1	Versal® ACAP	XCV1802-2MSELSVC4072 The heatsink is not shown in Figure 3¹	3-23
2	U25, U26	LPDDR4 16 GBIT comp. memory (B700-B702 IF)	Micron MT53D512M32D2DS-046 IC SDRAM LPDDR4 512Mx32 2133 MHz	3,39,40
3	U150, U151	LPDDR4 16 GBIT comp. memory (B703-B705 IF)	Micron MT53D512M32D2DS-046 IC SDRAM LPDDR4 512Mx32 2133 MHz	4,42,41
4	U246, U247	LPDDR4 16 GBIT comp. memory (B706-B708 IF)	Micron MT53D512M32D2DS-046 IC SDRAM LPDDR4 512Mx32 2133 MHz	5,43,44
5	J11	SYSMON header	Sullins PBC06DAAN Conn. hdr. vert. 12 pos. 2x6 2.54 mm pitch	20
6	J36	ACAP JTAG 2 mm 2x7 flat-cable connector	Molex 0878321420 Conn. hdr. male vert. 14 pos 2x7 2 mm	35
7	J332	Mictor-38 Arm® trace connector	TE connectivity AMP connectors 2-5767004-2 Conn. hdr. MICTOR 38 pos. 2x19 0.635 mm	38
8	J310	8A34001 I2C 2 mm 2x9 flat-cable connector	Molex 0878321820 Conn. hdr. male vert. 18 pos. 2x9 2 mm	111
9	J369, U20	USB-UART bridge, USB Type-C connector (USB2.0)	Amphenol 12401598E4#2A FTDI FT4232HL-REEL	36
10	J308, U99	USB 2.0 type-A connector, USB ULPI transceiver	Würth 629104190121, USB 2.0 type-A Microchip USB3320C USB 2.0 Xcvr	53
11	J302, U104	SD card socket, Versal ACAP SD 3.0 level translator circuit	Molex 5025700893 Micro SD card cage	51
12	U33, U35	I2C bus switches	Texas Instruments TCA9548APWR IC switch bus 1-In 8-Outs I2C 400 kHz Bottom of board	55,56
13	U233	I2C bus expander	Texas Instruments TCA6416APWR IC exp. GPIO 16-bit I2C 400 kHz Bottom of board	55
14	J1, J2, J354, J355, J358, J359	QSFP-DD 112G connector	Molex 2147334000 QSFP-DD 112G connector and cage	57-59
15	J350, J352, J385, J387	SFP-DD 56G connector	Molex 2047301000 SFP-DD 56G connector and cage	63,64

Table 2: Board Component Locations (cont'd)

Callout No.	Ref. Des.	Feature	Notes	Schematic Page
16	J307	GEM0 SGMII Ethernet PHY, 0x01, RJ45 w/mag	Halo HFJ11-1G01E-L12RL RJ-45 Gigabit connector	52
17	J51	FMCP1	Samtec ASP-184329-01 560 pos. connector 14x40 1.27 mm	46-50
18	Various	ACAP power management system (VCCINT, VCC_SOC)	Infineon regulators	67-73,75
19	U160, U293	VCC_PMC/PSFP/VCCO_MIO/ VCCAUX/VCC1V5/UTIL_3V3 regulator	Infineon IRPS5401MTRPBF IC PMU 5-Ch step-down DC/DC	76,77
20	U167, U294	VCCRAM_VCCINT/ LPDMGTAVCC/MGTVCCAUX/ MGTAVCC regulator	Infineon IRPS5401MTRPBF IC PMU 5-Ch step-down DC/DC	78,79
21	U175, U296	VCCAUX/UTIL_2V5/ VCC_PSLP_CPM5/ LPMGTAVCCAUX regulator	Infineon IRPS5401MTRPBF IC PMU 5-Ch step-down DC/DC	80,81
22	U295	UTIL_1V8/VCCAUX_PMC/ LPDMGTAVTT regulator	Infineon IRPS5401MTRPBF IC PMU 5-Ch step-down DC/DC	82
23	U259	LPDMGTAVTT regulator	Infineon IR38060MTRPBF IC REG BUCK ADJ 6A	85
24	U185	VADJ_FMC regulator	Infineon IR38164MTRPBFAUMA1 IC V. reg. step-down DC/DC sync	86
25	U187	VCC1V1_LP4 regulator	Infineon IR38164MTRPBFAUMA1 IC V. reg. step-down DC/DC sync	87
26	U189	MGTAVTT regulator	Infineon IR38164MTRPBFAUMA1 IC V. reg. step-down DC/DC sync	88
28	U191	UTIL_5V0 regulator	Infineon IR3889MTRPBFAUMA1 IC V. reg. step-down DC/DC sync	89
29	J325	PMBus 3-pin header	Sullins PBC03SAAN Conn. hdr. vert. 3 pos. 1x3 2.54 mm	55
30	Various	Power good LEDs (see Power and Status LEDs for more details)	Various; see the Bill of Materials	91
31	J16	Power connector, 2x3, for AC-DC power adapter	Molex 0039301060 Conn. ddr. RA 6 pos. 2x3 4.2 mm	66
32	JP1, JP2, JP3, JP4	Power connector, 2x4, for ATX PCIe power	Astron 6652208-T0003T-H Conn. hdr. male RA 8 pos. 2x4 4.2 mm	66
33	J233	Fan header (keyed 4-pin)	Molex 0470533000 Keyed fan header 4 pos. 0.100" vert.	66
34	U298, U299	MGT clock generators	Renesas RC21008A065GND#BB0	61,62
35	J370, J371	RC21008A_GTCLK1/2 header	Molex 0878321820	61,62
36	U11, U12	ACAP U1 QSPI	Micron MT25QU01GBBB8E12-OSIT IC flash NOR SPI 1 Gb	45
37	U32	ACAP U1 REF CLK, 33.33 MHz, 1.8V CMOS, 0x5D	Skyworks/Silicon Labs 570JAC000900DGR Osc. XO 10-280 MHz Bottom of board	54

Table 2: Board Component Locations (cont'd)

Callout No.	Ref. Des.	Feature	Notes	Schematic Page
38	U248	LPDDR4 CLK1, 200 MHz, 3.3V LVDS, 0x60	Skyworks/Silicon Labs 570BAB000299DGR Osc. XO 10-810 MHz Bottom of board	3
39	U3	LPDDR4 CLK2, 200 MHz, 3.3V LVDS, 0x60	Skyworks/Silicon Labs 570BAB000299DGR Osc. XO 10-810 MHz Bottom of board	4
40	U4	LPDDR4 CLK3, 200 MHz, 3.3V LVDS, 0x60	Skyworks/Silicon Labs 570BAB000299DGR Osc. XO 10-810 MHz Bottom of board	5
41	J373, J374, J375, J376, J393, J394, J395, J396	ACAP GTM female vertical 12.4 GHz SMT screw connector	Rosenberger 32K10K-400L5 Conn. rcpt. SMA vert. 50R 12.4 GHz	11
42	DS1	Done LED (Active-High-Z and pulled High)	Lumex SML-LX0603GW-TR LED green	22
43	DS2	Error out LED (Active-High-Z and pulled High)	Lumex SML-LX0603IW-TR LED red	22
44	DS3, DS4, DS5, DS6	User LEDs	Lumex SML-LX0603GW-TR LED green	65
45	U251, U252, U257	IEEE-1588 eCPRI input clock multiplexer	Renesas 8P3451204NLG18IC buffer Clk 2 to 4 1.8-2.5V 10 mA 1.5 GHz LVDS	113
46	U219	IEEE-1588 eCPRI CLK, various, 3.3V, 0x58	IDT 8A34001E-000AJG8 IC synch. man. unit 8-Ch 24 LVCMOS Bottom of board	111,112
47	J328, J329, J338	IEEE-1588 eCPRI 8A34001 CLK in SMA	Rosenberger 32K10K-400L5 Conn. rcpt. SMA vert. 50R 12.4 GHz	111
48	J330, J331, J339	IEEE-1588 eCPRI 8A34001 CLK out SMA	Rosenberger 32K10K-400L5 Conn. rcpt. SMA vert. 50R 12.4 GHz	111
49	U125	XCZU4EG system controller	Xilinx® XCZU4EG-2SFVC784E FPGA MPSoC Zynq UltraScale+	93-101
50	U319	SYSCTLR clocks 33.33 MHz and 26 MHz USB and 156.25 MHz HSDP REFCLK 0x6A	Skyworks/Silicon Labs Si5332FD10259-GM1 Low jitter clock generator with 6 outputs	108
51	U132	System controller LPDDR4 16 GBIT comp. memory	Micron MT53D512M32D2DS-046 WT:D IC SDRAM LPDDR4 16 Gb 512Mx32 2133 MHz	105
52	J349	System controller SGMII Ethernet, RJ45 w/magnetics	Halo HFJ11-1G01E-L12RL RJ-45 Gigabit connector	103
53	J7, U19	System controller USB 3.0 type-B connector, USB ULPI transceiver	Wurth 692622030100, USB 3.0 type-B Microchip USB3320C USB 2.0 Xcvr Bottom of board	107
54	DS34	System controller done LED (active-High)	Lumex SML-LX0603GW-TR LED green	97
55	J362	OSFP 112G connector	TE connectivity 2344064-4 OSFP 112G connector and cage	60

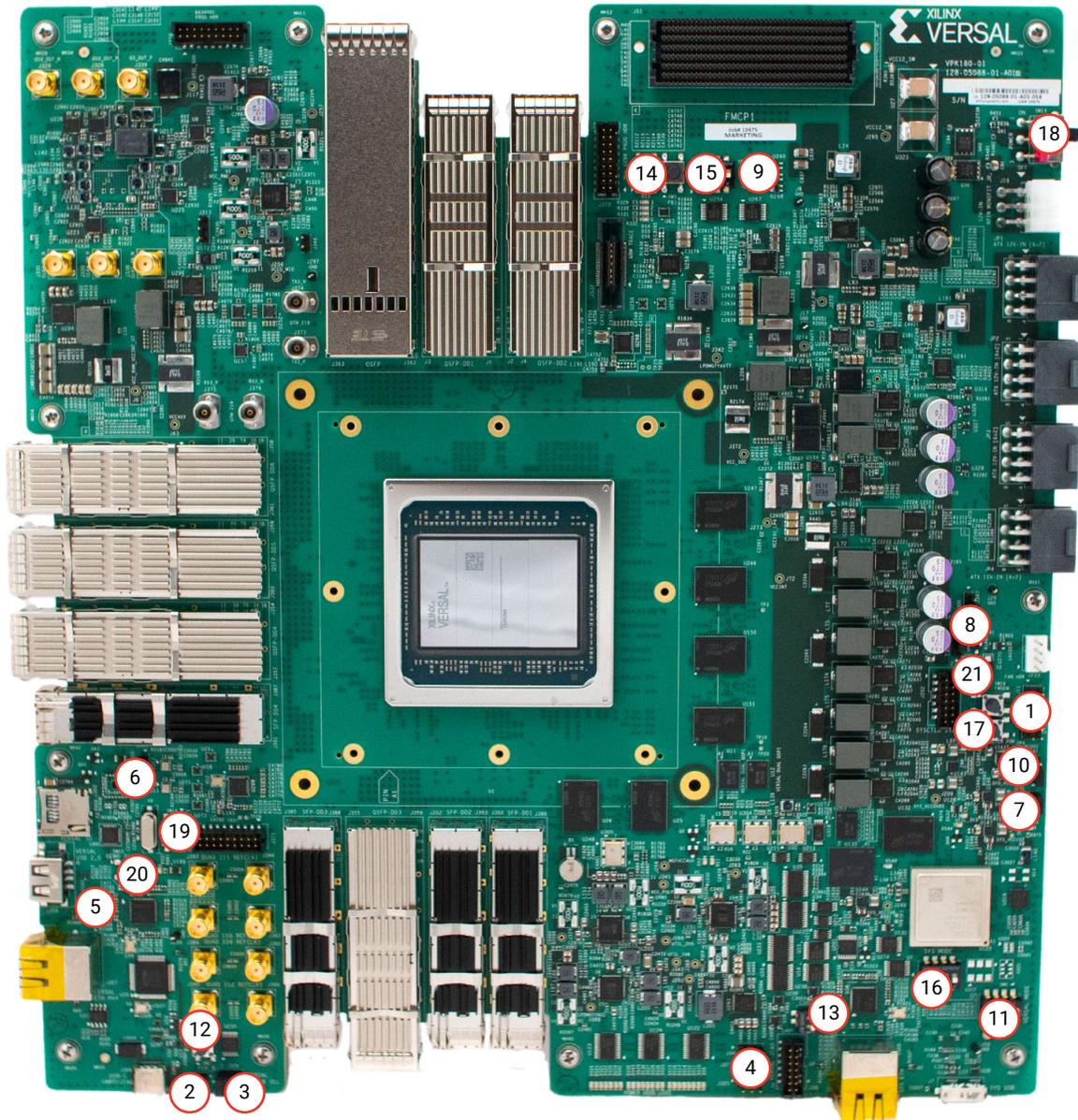
Notes:

- The VPK180 evaluation board includes a heatsink with a thermal resistance of 0.38°C/W.

Default Jumper and Switch Settings

The following figure shows the VPK180 board jumper header and switch locations. Each numbered component shown in the figure is keyed to the applicable table in this section. Both tables reference the respective schematic page numbers.

Figure 4: Board Jumper Header and Switch Locations



X27291-101322

Jumpers

The following table lists the default jumper settings.

Table 3: Default Jumper Settings

Callout Number	Ref. Des.	Function	Default	Schematic Page
1	J11	SYSMON VREFP SEL 1-2: External VREF 2-3: Disable external VREF	1-2	20
2	J26	POR_B supervisor SENSE input 1-2: VCCO_MIO ramp-up sense (1.8V) 2-3: VCCAUX_PMC ramp-up sense (1.5V)	1-2	23
3	J326	POR_B enable header 1-2: SYSCTLR can drive POR_B 3-4: PC4 can drive POR_B 5-6: FTDI can drive POR_B Open: POR_B source not connected	1-2, 3-4 jumpered 5-6 open	23
4	J34	VCC Fuse programming enable 1-2: Fuse programming enabled 2-3: Fuse programming disabled	2-3	25
4	J37	JTAG source enable 1-2: JTAG sources disabled 2-3: JTAG sources enabled	2-3	35
5	J300	USB shield GND 1-2: USB connector DC grounded 2-3: USB connector no DC grounded	1-2	53
6	J301	SD REF 1-2: 3.3V REF 2-3: GND REF	1-2	51
7	J203	SYSCTLR POR_B supervisor enable 1-2: SYSCTLR POR_B supervisor enabled Open: SYSCTLR POR_B supervisor disabled	1-2	97
8	J347	Fan type 1-2: System controller PWM 2-3: Versal ACAP MIO PWM	2-3	66
8	J348	TACH type 1-2: System controller TACH 2-3: Versal ACAP MIO TACH	2-3	66
9	J345	LPDMGTYAVTT enable select Installed: Versal ACAP control Not installed: enabled by UTIL_5V0_PGOOD	Open	90
10	J12	SYSMON VREF selection Default VREF = 1.024V	1-2	20

Switches

The following table lists the default switch settings.

Table 4: Default Switch Settings

Callout Number	Ref. Des.	Function	Default	Schematic Page
11	SW1	U1 mode 4-pole DIP switch Switch OFF = 1 = high; ON = 0 = low Mode = SW1[1:4] = Mode[0:3] SD = ON,OFF,OFF,OFF = 0111 QSPI32 = ON,OFF,ON,ON = 0100 JTAG = ON,ON,ON,ON = 0000	ON, ON, ON, ON	22
12	SW2	VPK180 power-on reset (POR_B)	Open	23
13	SW3	SYSCTLR JTAG source selection Switch OFF = 1 = high; ON = 0 = low SYSCTLR JTAG SOURCE SEL = SW3[1:2] = SEL[0:1] PL JTAG = ON,ON = 00 FTDI JTAG = OFF,ON = 10 Trace Mictor38 JTAG = ON,OFF = 01	OFF, ON	35
14	SW4, SW5	User pushbutton inputs Note: Pushbutton switch default = open = logic low (not pressed).	Open	65
15	SW6	User GPIO DIP Switch OFF = 0 = low; ON = 1 = high	OFF, OFF, OFF, OFF	65
16	SW11	SYSCTLR mode 4-pole DIP switch Switch OFF = 1 = high; ON = 0 = low Mode = SW1[1:4] = Mode[0:3] QSPI32 = ON,OFF,ON,ON = 0100 eMMC = ON,OFF,OFF,ON = 0110 JTAG = ON,ON,ON,ON = 0000	ON, OFF, ON, ON	97
17	SW12	System controller power-on reset (SYSCTL_POR_B)	Open	97
18	SW13	Main power	OFF	66
19	SW14	User USB reset	Open	53
20	SW15	User GEM reset	Open	52
21	SW16	System controller FWUEN pushbutton (SYSCTLR_MIO12_FWUEN_C2M_B) See BEAM wiki for more information	Open	96

Versal ACAP Configuration

The Versal XCVP1802 ACAP boot process is described in the “Platform Boot, Control, and Status” section of the *Versal ACAP Technical Reference Manual (AM011)*. The VPK180 board supports a subset of the modes documented in the technical reference manual via onboard boot options. The mode DIP switch SW1 configuration option settings are listed in the following table.

Table 5: Mode Switch SW1 Configuration Option Settings

Boot Mode	Mode Pins [0:3] ²	Mode SW1 [1:4] ²
JTAG	0000 ^{1,3}	ON, ON, ON, ON
QSPI32	0100	ON, OFF, ON, ON
SD1 (SD 3.0)	0111	ON, OFF, OFF, OFF

Notes:

1. Default switch setting.
2. Mode DIP SW1 poles [1:4] correspond to U1 XCVP1802 MODE[0:3].
3. Mode DIP SW1 individual switches ON=LOW (p/d to GND)=0, OFF=HIGH (p/u to VCCO)=1.

JTAG

The Vivado®, Xilinx SDK, or third-party tools can establish a JTAG connection to the Versal ACAP in the two ways described in this section.

- FTDI FT4232 USB-to-JTAG/USB-UART device (U20) connected to USB 2.0 type-C connector (J369), which requires:
 - Set boot mode SW1 for JTAG as indicated in the "Mode Switch SW1 Configuration Option Settings" table in [Versal ACAP Configuration](#).
 - On the 3-pin JTAG MUX, enable header J37 to enable the JTAG MUX. Move the 2-pin jumper to be installed on pins 2-3. See [Default Jumper and Switch Settings](#) for defaults and [Board Component Location](#) for location.
 - Set 2-pole DIP SW3[1:2] set to 10 (OFF, ON) for JTAG MUX channel 2 FT4232 U20 bridge.
 - Power-cycle the VPK180 evaluation board or press the power-on reset (POR) pushbutton (SW2). SW2 is near the USB-C JTAG port J369 in the figure in [Board Component Location](#).

- JTAG pod flat cable connector J36 (2 mm 2x7 shrouded/keyed), which requires:

Note: In this mode, the FT4232 device (U20) UART functionality continues to be available.

- Set boot mode SW1 for JTAG as indicated in the "Mode Switch SW1 Configuration Option Settings" table in [Versal ACAP Configuration](#).

- On the 3-pin JTAG MUX, enable header J37 to inhibit the JTAG MUX. Move the 2-pin jumper to be installed on pins 1-2 for high-z mode. See [Default Jumper and Switch Settings](#) for defaults and [Board Component Location](#) for location.
- 2-pole DIP SW3[1:2] setting does not matter as the MUX is inhibited/turned off.
- Power-cycle the VPK180 board or press the power-on reset pushbutton (SW2). SW2 is near the USB-C JTAG port J369 in the figure in [Board Component Location](#).

QSPI32

This boot mode is supported onboard and is wired to XCVP1802 U1 bank 500 PMC_MIO[0:12] pins. The supported QSPI configuration is dual-parallel x8. To boot from QSPI:

1. Store a valid XCVP1802 ACAP boot image file in the QSPI.
2. Set boot mode SW1 for QSPI32 as indicated in the "Mode Switch SW1 Configuration Option Settings" table in [Versal ACAP Configuration](#).
3. Power-cycle the VPK180 board or press the POR pushbutton SW2. SW2 is near the USB-C JTAG port J369 in the figure in [Board Component Location](#).

SD1_3.0

To boot from a SD card installed in microSD card socket J302:

1. Store a valid XCVP1802 ACAP boot image file on a microSD card. Plug the SD card into the VPK180 evaluation board SD socket J302 connected to the XCVP1802 U1 bank 501 MIO SD interface.
2. Set boot MODE SW1 for SD1_3.0 as indicated in the table in [Versal ACAP Configuration](#).
3. Power-cycle the VPK180 board or press the POR pushbutton SW2. SW2 is near the USB-C JTAG port J369 in the figure in [Board Component Location](#).

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. The "Board Component Locations" table in [Board Component Descriptions](#) identifies the components and references the respective schematic page numbers. Component locations are shown in the "Evaluation Board Component Locations" figure in [Board Component Location](#).

Component Descriptions

Versal ACAP

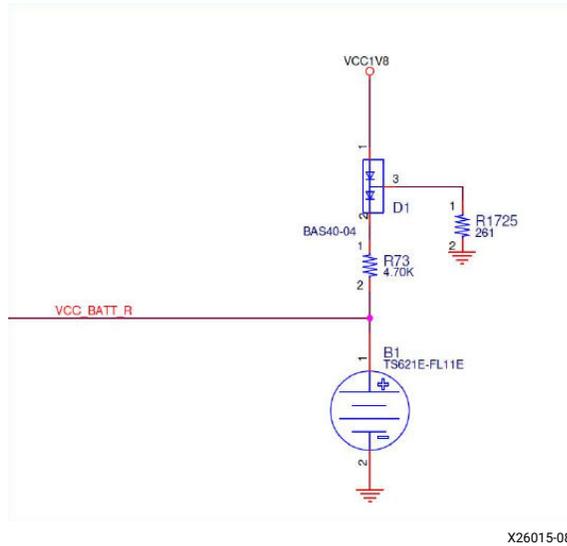
[[Figure 3](#), callout 1]

The VPK180 evaluation board is populated with the Versal® XCVP1802-2MSELSVC4072 ACAP, which combines a powerful processing system (PS) and programmable logic (PL) in the same device. The PS in a Versal ACAP features the Arm® flagship Cortex®-A72 64-bit dual-core processor and Cortex®-R5F dual-core real-time processor. For additional information on the Versal XCVP1802-2MSELSVC4072 ACAP, see the *Versal Premium Series Data Sheet: DC and AC Switching Characteristics* (DS959). See the *Versal ACAP Technical Reference Manual* ([AM011](#)) for more information about Versal ACAP configuration options.

Encryption Key Battery Backup Circuit

The XCVP1802 ACAP U1 implements bitstream encryption key technology. The VPK180 board provides the encryption key backup battery circuit shown in the following figure.

Figure 5: Encryption Key Backup Circuit



The Seiko TS621E rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCV1802 ACAP U1 VCC_BATT bank pin AN20. The battery supply current IBATT specification is 150 nA maximum when board power is off. Battery B1 is charged from the VCC1V8 1.8V rail through a 2 series diode with the first forward drop to yield between 0.24V to 0.46V over temperature per fixed 5 mA load, R1725, and limiting 1.56V max at the ACAP pin, PSVBATT. The second diode and 4.7 kΩ current limit resistor allows the battery to trickle charge and prevent battery B1 from back powering R1725.

I/O Voltage Rails

The XCV1802 ACAP PL I/O bank voltages on the VPK180 board are listed in the following table. See [LPD MIO\[23\]: VADJ_FMC Power Rail](#) for more details on the VADJ_FMC power rail.

Note: The VPK180 evaluation board is shipped with VCC_PMC set to 0.88V, allowing for overdrive. See the *Versal Premium Series Data Sheet: DC and AC Switching Characteristics (DS959)* for more information. See the *Versal ACAP Technical Reference Manual (AM011)* for more information about Versal ACAP configuration options.

Table 6: I/O Voltage Rails

ACAP (U1) Bank	Power Supply Rail Net Name	Voltage	Description
XPIO Bank 700	VCC1V1_LP4	1.1V	LPDDR4 TRIP1 CH1
XPIO Bank 701	VCC1V1_LP4	1.1V	LPDDR4 TRIP1 CH0, LPDDR4 TRIP1 CH1
XPIO Bank 702	VCC1V1_LP4	1.1V	LPDDR4 TRIP1 CH0
XPIO Bank 703	VCC1V1_LP4	1.1V	LPDDR4 TRIP2 CH1
XPIO Bank 704	VCC1V1_LP4	1.1V	LPDDR4 TRIP2 CH0, LPDDR4 TRIP2 CH1
XPIO Bank 705	VCC1V1_LP4	1.1V	LPDDR4 TRIP2 CH0

Table 6: I/O Voltage Rails (cont'd)

ACAP (U1) Bank	Power Supply Rail Net Name	Voltage	Description
XPIO Bank 706	VCC1V1_LP4	1.1V	LPDDR4 TRIP3 CH1
XPIO Bank 707	VCC1V1_LP4	1.1V	LPDDR4 TRIP3 CH0, LPDDR4 TRIP3 CH1
XPIO Bank 708	VCC1V1_LP4	1.1V	LPDDR4 TRIP3 CH0
XPIO Bank 709	VADJ_FMC ¹	1.5V (default)	FMCP1_LA[17:18]_CC, FMCP1_LA[19:33], FMCP1_SYNC, FMCP_CLK1, SFPDD[1:2] I/O
XPIO Bank 710	VADJ_FMC ¹	1.5V (default)	FMCP1_LA[00:01]_CC, FMCP1_LA[02:16], FMCP1_CLK0, SFPDD[3:4] I/O
XPIO Bank 711	VCC1V5	1.5V	8A34001_GPIO_[14:15], SYSCTLR_GPIO[0:15], QSFDD[1:6] I/O, GPIO_PB[0:1]
XPIO Bank 712	VCC1V5	1.5V	GPIO_DIP_SW[0:3], GPIO_LED_[0:3]_LS, UART1, OSFP control signals, TRACE signals, 8A34001_GPIO[0:7;10:13]
PMC MIO 500	VCCO_MIO	1.8V	SYSMON, USB ULPI 2.0 interface, QSPI1/2 interface
PMC MIO 501	VCCO_MIO	1.8V	SD bus power, I2C0/21, UART0, System Controller I2C/trigger, SD card controls, GEM reset
LPD MIO 502	VCCO_502	1.8V	GEM interface/controls, power enables, fan tach, fan PWM

Notes:

1. The VPK180 board is shipped with VADJ_FMC set to 1.5V by the ZU4 system controller.

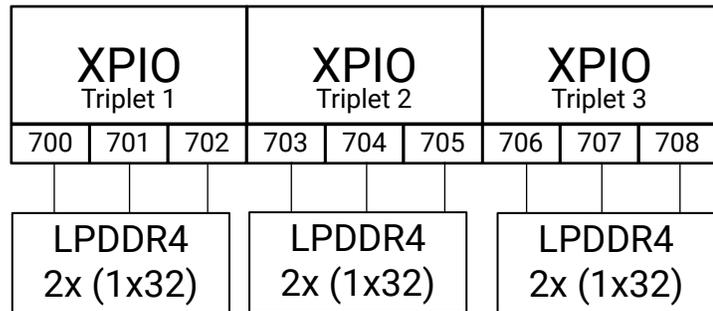
LPDDR4 Component Memory

[Figure 3, callout 2, 3, 4]

The VPK180 XCVP1802 ACAP PL DDR memory interface performance is documented in the *Versal Premium Series Data Sheet: DC and AC Switching Characteristics (DS959)*. The VPK180 board LPDDR4 component memory interfaces adhere to the constraints guidelines documented in the "PCB guidelines for Memory Interfaces" section of the *Versal ACAP PCB Design User Guide (UG863)*. The VPK180 DDR4 component interface is a 40Ω impedance implementation. Other memory interface details are also available in the *Versal ACAP Memory Resources Architecture Manual (AM007)*. For more memory component details, see the Micron MT53D512M32D2DS data sheet on the [Micron](#) website. For the most current part number, see the Bill of Materials (BOM) located on the [VPK180 Evaluation Board](#) website. The detailed ACAP connections for the feature described in this section are documented in the VPK180 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

The VPK180 evaluation board hosts three LPDDR4 memory systems, each with a component configuration of 2x (1x32-bit component).

Figure 6: LPDDR4 Component Memory



X26003-080522

XCVP1802 U1 has been configured with three triplet banks.

- XPIO triplet 1 (banks 700/701/702)
- XPIO triplet 2 (banks 703/704/705)
- XPIO triplet 3 (banks 706/707/708)

Each support two independent 32-bit 2 GB component interfaces (4 GB per triplet). The VPK180 evaluation board uses the LPDDR4 memory components as follows:

- Manufacturer: Micron
- Part number: MT53D512M32D2DS-046 WT:D (dual die LPDDR4 SRAM)
- Component description
 - 16 Gb (512 Mb x 32)
 - 1.1V 200-ball WFBGA
 - DDR4-2133

The VPK180 XCVP1802 ACAP PL DDR interface performance is documented in the *Versal Premium Series Data Sheet: DC and AC Switching Characteristics* (DS959). The VPK180 evaluation board LPDDR4 component memory interfaces adhere to the constraints guidelines documented in the PCB guidelines for the DDR4 section of the *Versal ACAP PCB Design User Guide* (UG863). The VPK180 DDR4 component interface is a 40Ω impedance implementation. Other memory interface details are also available in the *Versal ACAP Memory Resources Architecture Manual* (AM007). For more memory component details, see the Micron MT53D512M32D2DS data sheet at the [Micron website](#). The detailed ACAP connections for the feature described in this section are documented in the VPK180 evaluation board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

System Reset POR_B

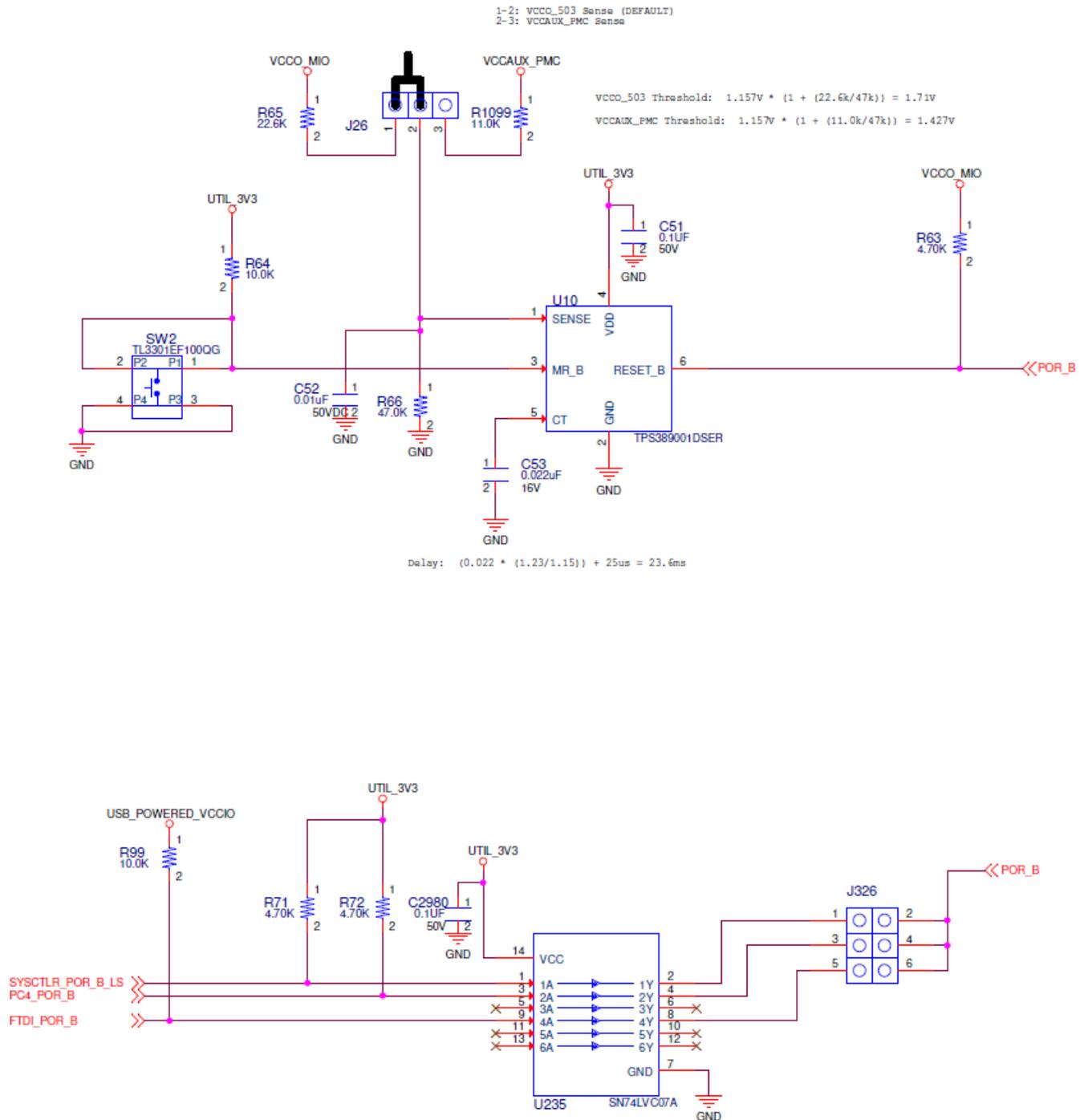
[Figure 4, callout 2]

POR_B is the Versal ACAP processor reset, which can be controlled by:

- SYSCTLR (U125)
- PC4 header (J36)
- FTDI USB JTAG chip (U20)

In the following figure, U235 allows directional open drain level shifting for all of these masters, and J326 allows them to be bused together if desired. The TPS389001 U10 supervisor chip holds POR_B off until power is valid. The VPK180 board POR circuit is shown in the following figure.

Figure 7: POR_B Reset Circuit



X26016-111821

PMC and LPD MIO

The following sections provide the MIO peripheral mapping implemented on the VPK180 evaluation board. See the *Versal ACAP Technical Reference Manual* ([AM011](#)) for more information on MIO peripheral mapping. Additional signal connectivity can be located in the following schematic sections:

- Bank 500: See schematic page 20
- Bank 501: See schematic page 21
- Bank 502: See schematic page 21

The following table provides MIO peripheral mapping implemented on the VPK180 evaluation board. The ACAP bank 500, 501, and 502 mappings are listed in the following table.

Table 7: MIO Peripheral Mapping

Bank	MIO #	Device	Signal	I/O	Notes
500	0	QSPI	PMC_MIO0_QSPI_CLK	I/O	
	1		PMC_MIO1_QSPI_DQ1	I/O	
	2		PMC_MIO2_QSPI_DQ2	I/O	
	3		PMC_MIO3_QSPI_DQ3	I/O	
	4		PMC_MIO4_QSPI_DQ0	I/O	
	5		PMC_MIO5_QSPI_CS_B	I/O	
	6		(Reserved for QSPI LOOPBACK)		Not routed on the PCB
	7		PMC_MIO7_QSPI_CS_B	I/O	
	8		PMC_MIO8_QSPI_DQ0	I/O	
	9		PMC_MIO9_QSPI_DQ1	I/O	
	10		PMC_MIO10_QSPI_DQ2	I/O	
	11		PMC_MIO11_QSPI_DQ3	I/O	
	12		PMC_MIO12_QSPI_CLK	I/O	
	13	USB	PMC_MIO13_USB_RST_B	O	USB RESET_B
	14		PMC_MIO14_USB_DAT0	I/O	USB Data0
	15		PMC_MIO15_USB_DAT1	I/O	USB Data1
	16		PMC_MIO16_USB_DAT2	I/O	USB Data2
	17		PMC_MIO17_USB_DAT3	I/O	USB Data3
	18		PMC_MIO18_USB_CLKOUT	I/O	USB CLKOUT
	19		PMC_MIO19_USB_DAT4	I/O	USB Data4
	20		PMC_MIO20_USB_DAT5	I/O	USB Data5
	21		PMC_MIO21_USB_DAT6	I/O	USB Data6
	22		PMC_MIO22_USB_DAT7	I/O	USB Data7
	23		PMC_MIO23_USB_DIR	I/O	USB DIR
	24		PMC_MIO24_USB_STP	O	USB STP
	25		PMC_MIO25_USB_NXT	I/O	USB NXT

Table 7: MIO Peripheral Mapping (cont'd)

Bank	MIO #	Device	Signal	I/O	Notes
501	26	SD	PMC_MIO26_SD_CLK	O	SD CLK
	27		PMC_MIO27_SD_DIR1	O	SD CLK
	28		PMC_MIO28_SD_DET	I	SD DETECT
	29		PMC_MIO29_SD_CMD	I/O	SD CMD
	30		PMC_MIO30_SD_DAT0	I/O	SD DAT0
	31		PMC_MIO31_SD_DAT1	I/O	SD DAT1
	32		PMC_MIO32_SD_DAT2	I/O	SD DAT2
	33		PMC_MIO33_SD_DAT3	I/O	SD DAT3
	34		PMC_MIO34_SD_SEL	I/O	SD SEL
	35		PMC_MIO35_SD_DIR_CMD	O	SD DIR_CMD
	36		PMC_MIO36_SD_DIR0	O	SD DIR0
	37		SYSCTLR	PMC_MIO37_501_ZU4_TRIGGER	I/O
	38				
	39	SYSMON I2C	PMC_MIO39_SYSMON_I2C_SCL	I/O	SYSMON I2C SCL
	40		PMC_MIO40_SYSMON_I2C_SDA	I/O	SYSMON I2C SDA
	41		PMC_MIO41_SYSMON_I2C_ALERT	I/O	SYSMON_I2C_ALERT
	42	UART	PMC_MIO42_501_RX_IN	I	UART RX
	43		PMC_MIO43_501_TX_OUT	O	UART TX
	44	I2C1	PMC_MIO44_501_LP_I2C1_SCL	I/O	I2C1 SCL
	45		PMC_MIO45_501_LP_I2C1_SDA	I/O	I2C1 SDA
	46	I2C0	PMC_MIO46_501_I2C0_SCL	I/O	I2C0 SCL
	47		PMC_MIO47_501_I2C0_SDA	I/O	I2C0 SDA
	48		PMC_MIO48_501	O	GEM0 RESET
	49	Regulator Enable GPIO	VCC_PSLP_EN_LS	O	PSLP Power Enable
	50				
	51	SD	PMC_MIO51_SD_BUSPWR	O	SD BUSPWR

Table 7: MIO Peripheral Mapping (cont'd)

Bank	MIO #	Device	Signal	I/O	Notes
502	0	GEM0	LPD_MIO0_GEM_TX_CLK	O	GEM_TX_CLK
	1		LPD_MIO1_GEM_TX_D0	I/O	GEM_TX_D0
	2		LPD_MIO2_GEM_TX_D1	I/O	GEM_TX_D1
	3		LPD_MIO3_GEM_TX_D2	I/O	GEM_TX_D2
	4		LPD_MIO4_GEM_TX_D3	I/O	GEM_TX_D3
	5		LPD_MIO5_GEM_TX_CTL	I/O	GEM_TX_CTL
	6		LPD_MIO6_GEM_RX_CLK	I	GEM_RX_CLK
	7		LPD_MIO7_GEM_RX_D0	I/O	GEM_RX_D0
	8		LPD_MIO8_GEM_RX_D1	I/O	GEM_RX_D1
	9		LPD_MIO9_GEM_RX_D2	I/O	GEM_RX_D2
	10		LPD_MIO10_GEM_RX_D3	I/O	GEM_RX_D3
	11		LPD_MIO11_GEM_RX_CTL	I/O	GEM_RX_CTL
	12				
	13	Regulator Enable GPIO	VCC_SOC_EN_LS	O	VCC_SOC Power Enable
	14				
	15	Regulator Enable GPIO	VCC_PSFP_EN_LS	O	VCC_PSFP Power Enable
	16	Regulator Enable GPIO	VCC1V1_LP4_AUX_EN_LS	O	VCC1V1, Aux Power Enable
	17				
	18				
	19				
	20	Regulator Enable GPIO	VCC_PL_EN_LS	O	VCC PL Power Enable
	21	FAN	MIO21_FAN_PWM_VERSAL	O	Versal ACAP Fan PWM
	22		MIO22_FAN_TACH_VERSAL	I	Versal ACAP Fan Tach
	23	Regulator Enable GPIO	VADJ_FMC_EN_LS	O	VADJ_FMC Enable
	24	MDIO	LPD_MIO24_GEM_MDC	O	GEM MD Clock
25	LPD_MIO24_GEM_MDIO		I/O	GEM MD I/O	

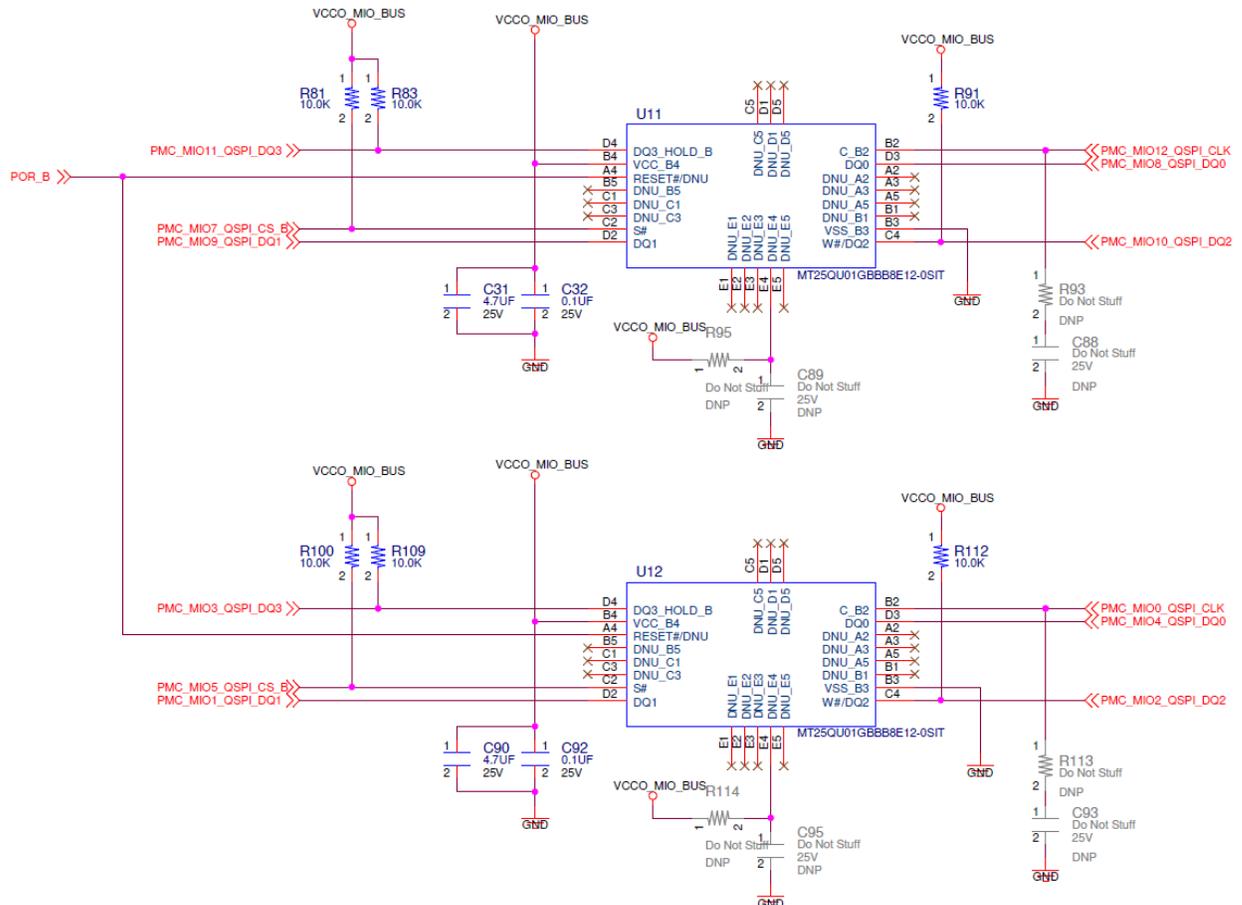
PMC MIO[0–12] Bank 500: QSPI U11, U12

[Figure 3, callout 36]

The VPK180 evaluation board uses two Micron MT25QU01GBBB8E12-0SIT 4-bit serial peripheral interface (quad SPI) flash devices. These 1 Gb NOR flash devices are organized in a dual parallel configuration and can be used as onboard boot, as well as non-volatile storage memory. When used as a boot source, it is selectable from SW1. See [Switches](#) for more information.

See schematic pages 12 and 33.

Figure 8: Dual Parallel QSPI Circuit



X26295-021422

PMC MIO[13:25] Bank 500: USB 2.0 ULPI PHY

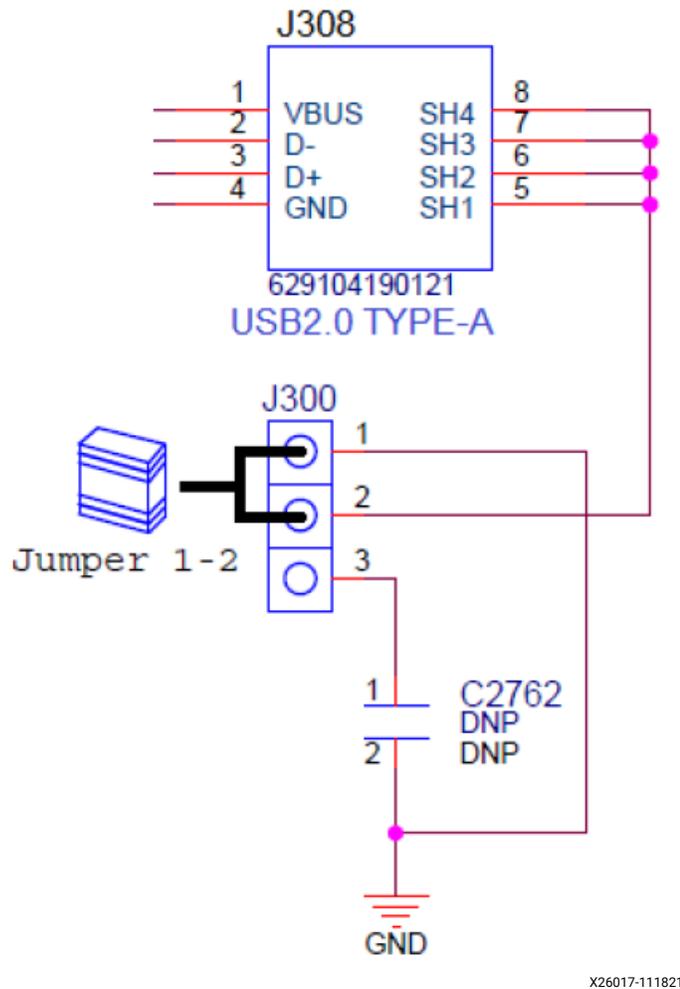
The VPK180 evaluation board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI transceiver (U99) to support a USB 2.0 type-A connector (J308). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device, which drives the physical USB signaling. Using the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

The USB3320 is clocked by a 24 MHz crystal (X8). See the [Standard Microsystems Corporation \(SMSC\) USB3320 data sheet](#) for clocking mode details. The interface to the USB3320 PHY is implemented through the IP in the XCVP1802 ACAP PS.

The USB3320 ULPI transceiver circuit has a Micrel MIC2544 high-side programmable current limit switch (U100). This switch has an open-drain output fault flag on pin 2, which turns on red LED DS37 if over current or thermal shutdown conditions are detected.

Note: As shown in the following figure, the shield for the USB 2.0 type-A connector (J308) can be tied to GND by a jumper on header J300 pins 1-2 (see [Default Jumper and Switch Settings](#)). The USB shield can optionally be connected through a series capacitor to GND by installing a capacitor (body size 0402) at location C2762 and inserting a jumper across pins 2-3 on header J300.

Figure 9: USB3320 USB2.0 Connector J308 Shield Connection Options



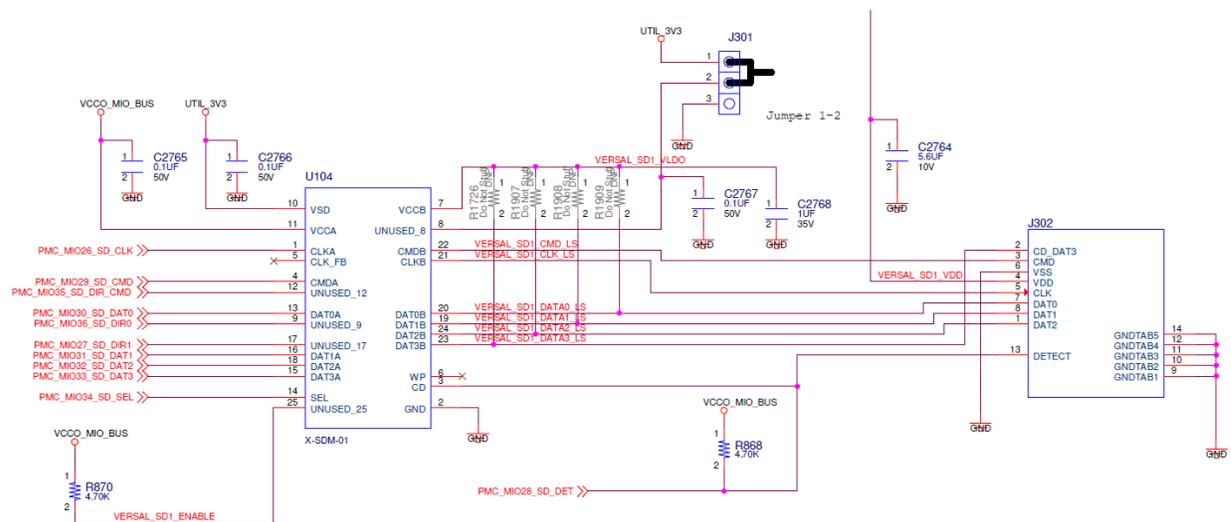
PMC MIO[26:36, 51] Bank 501: Secure Digital (SD) Card IF

[Figure 3, callout 11]

The VPK180 evaluation board includes a secure digital input/output (SDIO) interface to provide access to general purpose non-volatile SDIO memory cards and peripherals. This interface is used for the SD boot mode and supports SD2.0 and SD3.0 access.

The SDIO interface signals PMC_MIO[26:36, 51] are connected to XCVP1802 ACAP bank 501, which has its VCCO set to 1.8V. Six SD interface nets PMC_MIO[26, 29, 30:33] are passed through a NXP NVT4857UK SD 3.0-compliant voltage level-translator U104. This translator is present between the Versal ACAP and the SD card connector (J302). The NXP NVT4857UK U104 device provides SD3.0 capability with SDR104 performance. The following figure shows the connections of the SD card interface on the VPK180 evaluation board.

Figure 10: SD Card Interface Connections



X26058-120921

The following table lists the NVT4857UK U104 adapter pinout.

Table 8: NVT4857UK U104 Adapter Pinout

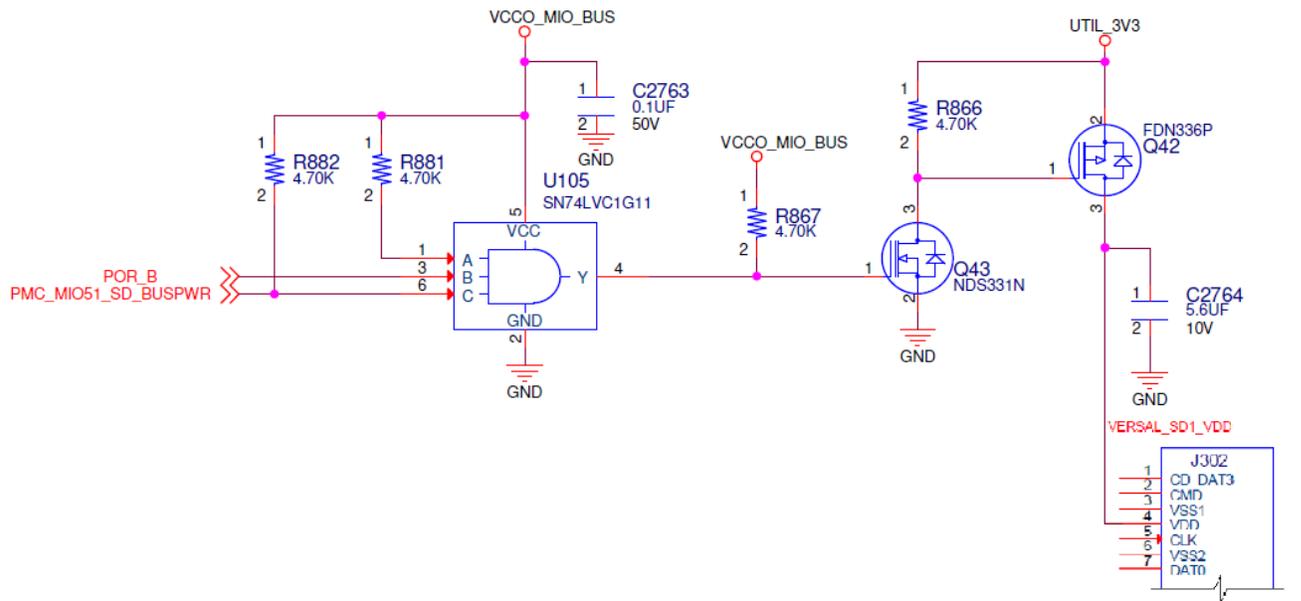
Aries Adapter Pin Number	NVT4857UKAZ Pin Number	NVT4857UKAZ Pin Name
1	D2	CLKA
2	C3, C2	GND
3	B2	CD
4	C1	CMDA
5	E2	CLK_FB
6	Unused	Unused
7	B3	VCCB
8	Unused	Unused
9	Unused	Unused
10	A3	VSD
11	A2	VCCA

Table 8: NVT4857UK U104 Adapter Pinout (cont'd)

Aries Adapter Pin Number	NVT4857UKAZ Pin Number	NVT4857UKAZ Pin Name
12	Unused	Unused
13	D1	DATA0
14	E3	SEL
15	B1	DAT3A
16	E1	DAT1A
17	Unused	Unused
18	A1	DAT2A
19	E4	DAT1B
20	D4	DAT0B
21	D3	CLKB
22	C4	CMDB
23	B4	DAT3B
24	A4	DAT2B
25	Unused	Unused

The ACAP (U1) also has control over the power for the SDCARD, which allows the ACAP to remove power to the SD card as needed.

Figure 11: SD Socket J302 Power Control



X26018-111821

Information for the SD I/O card specification can be found at the [SanDisk Corporation](#) or [SD Association](#) websites. The VPK180 SD card interface supports the SD1 (2.0) and SD2 (3.0) configuration boot modes documented in the *Versal ACAP Technical Reference Manual (AM011)*. See schematic page 51 for more details.

For NVP NVT4857UK component details, see the NVT4857UK data sheet on the [NXP](#) website.

The detailed ACAP connections for the feature described in this section are documented in the VPK180 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

PS MIO[37] Reserved

The ACAP PS bank 501 MIO37 is factory reserved.

PMC MIO[39:41] System Monitor I2C

The ACAP PS bank 501 MIO39 (PMC_MIO39_SYSMON_I2C_SCL), MIO40 (PMC_MIO40_SYSMON_I2C_SDA), and MIO41 (PMC_MIO41_SYSMON_I2C_ALERT) are connected to the system controller for use with the system controller related applications and alerts.

PMC MIO[42:43] UART0

[[Figure 3](#), callout 9]

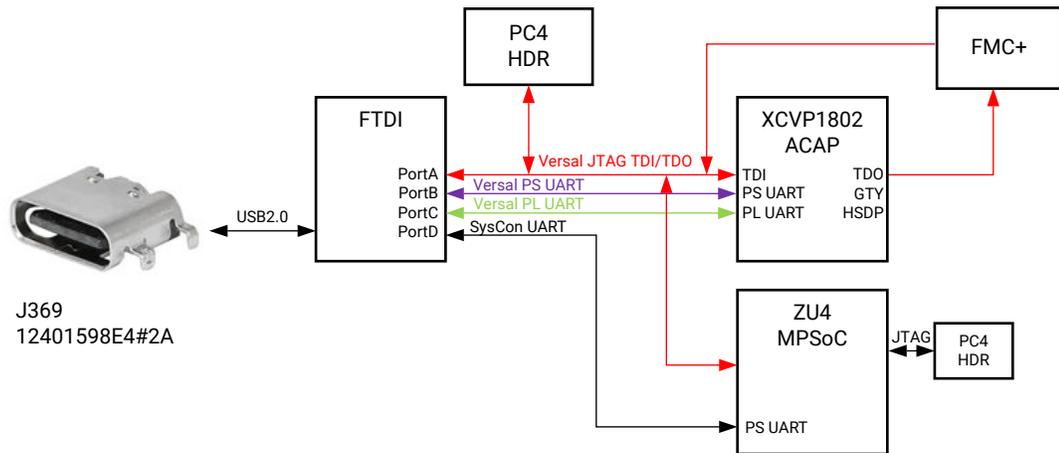
This is the primary Versal ACAP PS-side UART interface. MIO42 (RX_IN) and MIO43 (TX_OUT) are connected to FTDI FT4232HL U20 USB-to-Quad-UART bridge port BD through TI SN74AVC4T245 level-shifters U18 and U271. The FT4232HL U20 port assignments are listed in the following table.

Table 9: FT4232HL Port Assignments

FT4232HL U34	Versal ACAP U1
Port AD JTAG	VPK180 JTAG chain
Port BD UART0	PS_UART0 (MIO 42-43)
Port CD UART1	PL_UART1 bank 712
Port DD UART2	U20 system controller UART

The FT4232HL UART interface connections are shown in the following figure.

Figure 12: FT4232HL UART Connections



X26551-102722

For more information on the FT4232HL, see the [Future Technology Devices International Ltd.](https://www.future-technology.com/) website.

Note: This FTDI configuration image is not provided nor supported. To replicate this feature, a JTAG-SMT2 from [Digilent](https://www.digilent.com/) or similar is recommended.

The detailed ACAP connections for the feature described in this section are documented in the VPK180 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

PMC MIO[44:45] I2C1 Bus

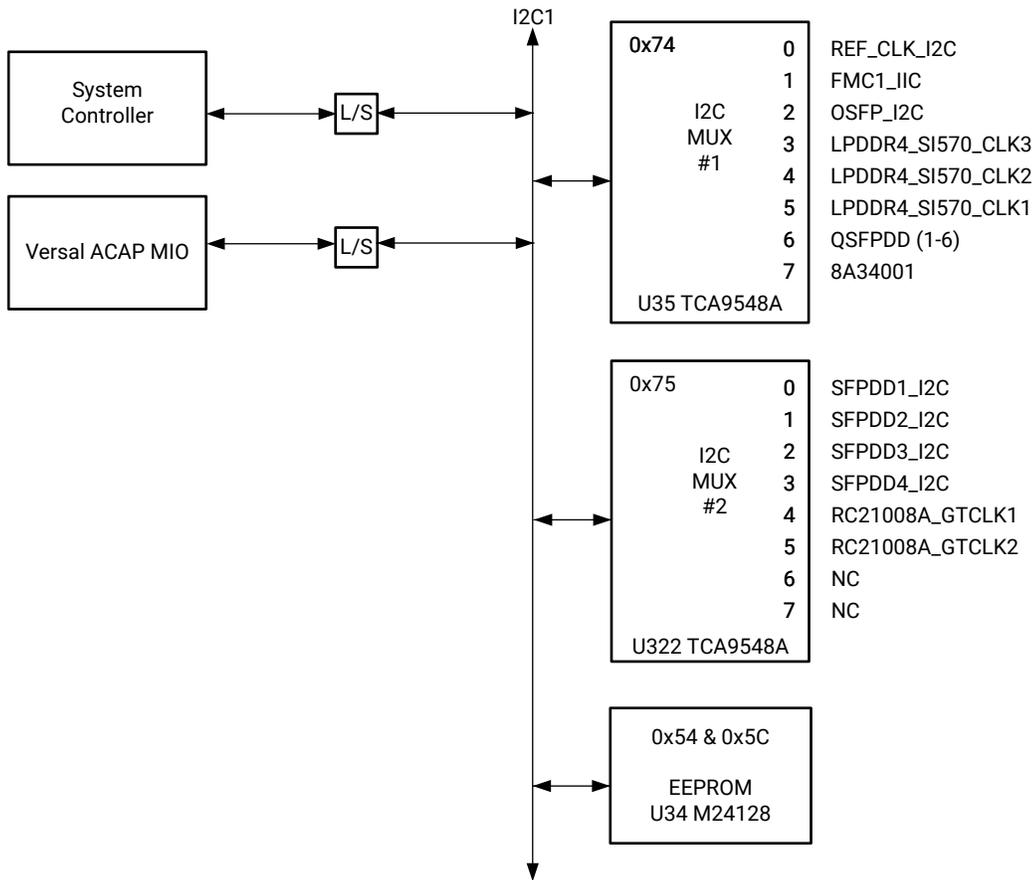
[[Figure 3](#), callout 12]

Bus I2C1 connects the XCV1802 U1 PS bank 501 and the XCZU4EG system controller U125 PS bank 501 to two I2C switches (TCA9548A U35 and U322). These I2C1 connections enable I2C communications with other I2C capable target devices. TCA9548A U35 is pin-strapped to respond to I2C address $0x74$. TCA9548A U322 is pin-strapped to respond to I2C address $0x75$. The following figure shows the I2C1 bus connectivity detailed in the table below.

Details for controlling the U35 and U322 TCA9548A switches are available in the data sheet on the [Texas Instruments](https://www.ti.com/) website.

The detailed ACAP connections for the feature described in this section are documented in the VPK180 evaluation board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

Figure 13: I2C1 Bus Topology



X26552-071922

U34 is an I2C addressable 128-Kbit serial I2C bus EEPROM. It has two addresses associated with it and is connected at the same I2C level as the I2C multiplexer listed in the following table. Address 0x54 is used when the memory array is accessed. When using 0x5C, the identification page is accessed.

The U35 and U322 addresses 0x74 and 0x75 connections are listed in the following tables.

Table 10: I2C1 Multiplexer TCA9548A U35 Address 0x74 Connections

I2C Devices	I2C MUX Pos.	I2C Address	Devices
REF_CLK_I2C	0	0x5D	U32
FMC1_IIC	1	0x##	J51
OSFP_I2C	2	0x##	J362
LPDDR4_SI570_CLK3	3	0x60	U4
LPDDR4_SI570_CLK2	4	0x60	U3
LPDDR4_SI570_CLK1	5	0x60	U248
QSFPDD (1-6)	6	0x##	J1, J2, J354, J355, J358, J359

Table 10: I2C1 Multiplexer TCA9548A U35 Address 0x74 Connections (cont'd)

I2C Devices	I2C MUX Pos.	I2C Address	Devices
8A34001	7	0x5B	U219, J310

Table 11: I2C1 Multiplexer TCA9548A U322 Address 0x75 Connections

I2C Devices	I2C MUX Pos.	I2C Address	Devices
SFPDD1_I2C	0	0x##	J350
SFPDD2_I2C	1	0x##	J352
SFPDD3_I2C	2	0x##	J385
SFPDD4_I2C	3	0x##	J387
RC21008A_GTCLK1	4	0x09	U298
RC21008A_GTCLK2	5	0x09	U299

PMC MIO[46:47] I2C0 Bus

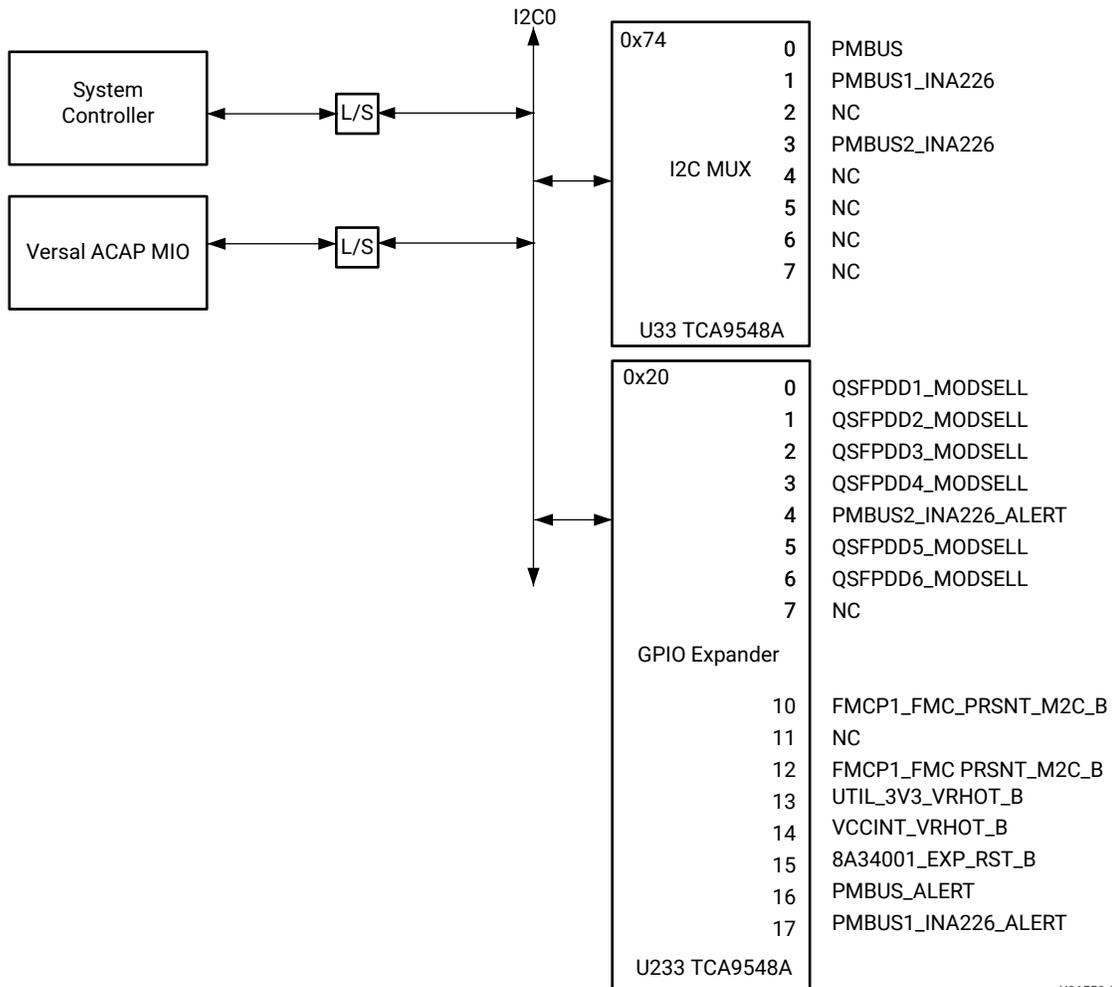
[Figure 3, callout 12]

Bus I2C0 connects the XCVP1802 U1 PS bank 501 and the XCZU4EG system controller U125 PS bank 501 to a GPIO 16-bit port expander (TCA6416A U233) and I2C switch (TCA9548A U33). The port expander enables accepting various fan controller, FMCP connector, and power system status inputs. Bus I2C0 also provides access to power system PMBus power controllers and INA226 power monitors, as well as three SI570 components via the U33 TCA9548A switch. TCA6416A U233 is pin-strapped to respond to I2C address 0x20. The TCA9548A U33 switch is set to 0x74. Details for controlling the U33 TCA9548A switch can be located in the data sheet located on the [Texas Instruments](https://www.ti.com) website.

The detailed ACAP connections for the feature described in this section are documented in the VPK180 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

The following figure shows the I2C0 bus connectivity.

Figure 14: I2C0 Bus Topology



X26553-071922

The devices on each port of the I2C0 U233 TCA6416A port expander and on each bus of the I2C0 U33 TCA9548A switch are listed in the following tables.

Table 12: I2C0 Port Expander TCA6416A U233 Address 0x20 Connections

I2C Devices	Port	Direction	Device
QSFDD1_MODSELL	P00	Out	J1 QSFP-DD
QSFDD2_MODSELL	P01	Out	J2 QSFP-DD
QSFDD3_MODSELL	P02	Out	J355 QSDP-DD
QSFDD4_MODSELL	P03	Out	J354 QSDP-DD
PMBUS2_INA226_ALERT	P04	In	U125 (ZU4), U166, U168, U172, U174, U176, U177, U184, U186, U188, U234, U260, U264, U265
QSFDD5_MODSELL	P05	Out	J359 QSDP-DD
QSFDD6_MODSELL	P06	Out	J358 QSFP-DD
NC	P07-P09	N/A	N/A

Table 12: I2C0 Port Expander TCA6416A U233 Address 0x20 Connections (cont'd)

I2C Devices	Port	Direction	Device
FMCP1_FMC_PRSNT_M2C_B	P10	In	J51 FMCP HSPC
NC	P11	N/A	N/A
FMCP1_FMCP_PRSNT_M2C_B	P12	In	J51 FMCP HSPC
UTIL_3V3_VRHOT_B	P13	N/A	N/A
VCCINT_VRHOT_B	P14	In	U152 IR35215
8A34001_EXP_RST_B	P15	Out	U221 SN74LVC1G08
PMBUS_ALERT	P16	In	U125 (ZU4), U152, U160, U167, U175, U185, U187, U189, U259, U291, U295
PMBUS1_INA226_ALERT	P17	In	U5, U65, U125 (ZU4), U161, U163, U164, U165

Table 13: I2C0 Multiplexer TCA9548A U33 Address 0x74 Connections

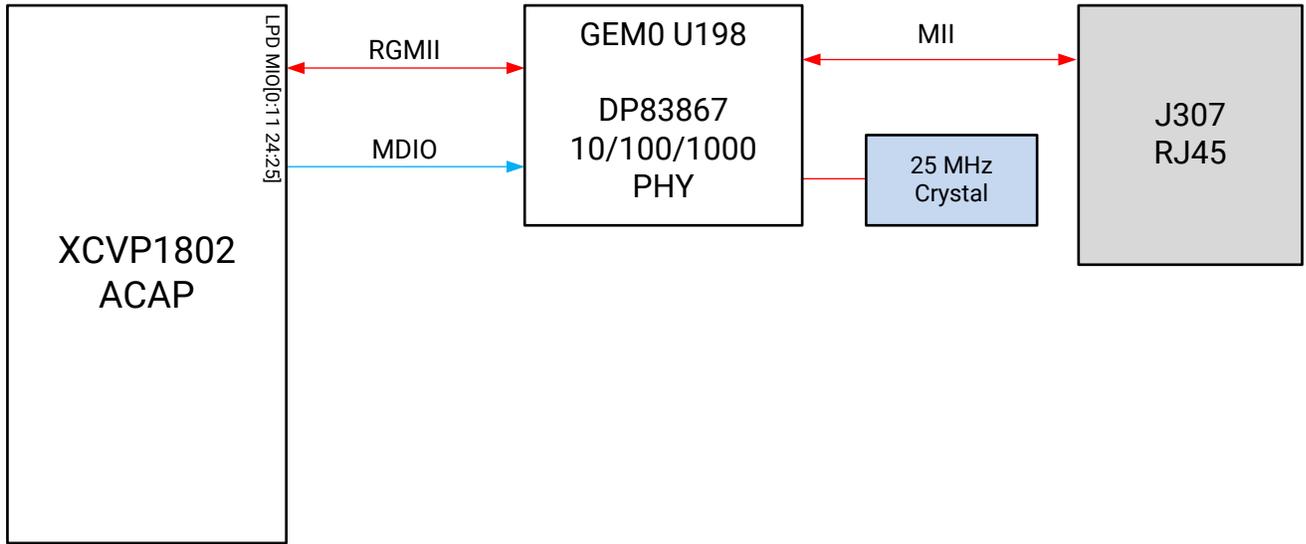
I2C Devices	I2C Switch Pos.	I2C Address	Devices
PMBUS	0		See Board Power System
PMBUS1_INA226	1		See Board Power System
NC	2		N/A
PMBUS2_INA226	3		See Board Power System
NC	4		N/A
NC	5		N/A
NC	6		N/A
NC	7		N/A

PMC MIO[48] and LPD_MIO[0:11, 24:25]: GEM0 Ethernet

[[Figure 3](#), callout 16]

A PS Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface. In the following figure, ACAP (U1) is connected to TI DP83867 U198 Ethernet RGMII PHY before being routed to an RJ45 Ethernet connector J307. The RGMII Ethernet PHY is boot strapped to PHY address (0x01) and Auto Negotiation is set to Enable.

Figure 15: RGMII Ethernet



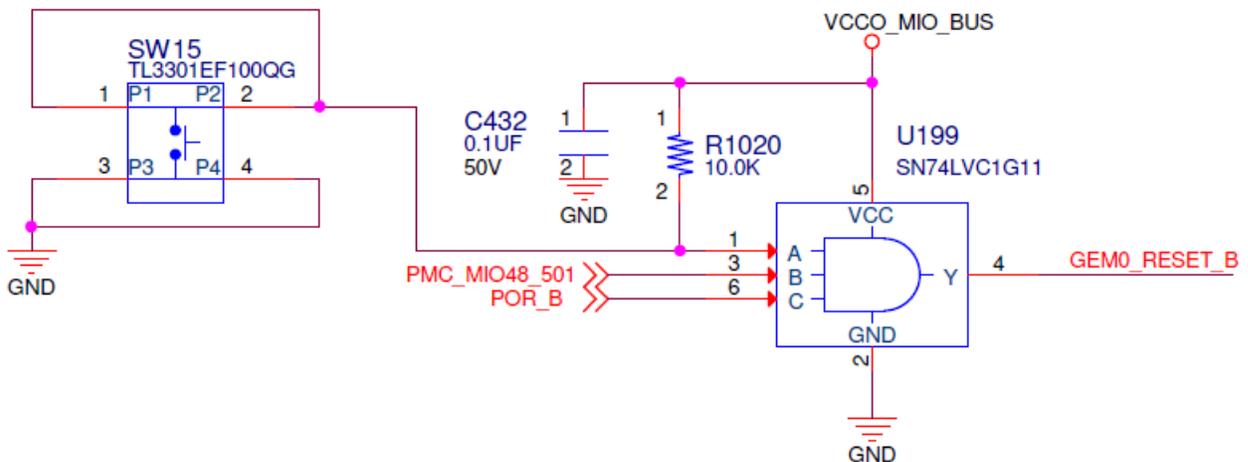
X27353-102722

Ethernet PHY (Three Resets)

[Figure 3, callout 16]

The DP83867 PHY (GEM0 U198) is reset by its GEM0_RESET_B generated by dedicated pushbutton switch (SW15) and PMC_MIO signals as shown in the following figure. The POR_B signal generated by the TPS389001DSER U10 POR device is wired in parallel to each Ethernet PHY reset circuit. The POR device is activated by pushbutton SW2. See [System Reset POR_B](#) for more details.

Figure 16: Ethernet PHY Reset Circuit



X26024-111821

Ethernet PHY LED Interface

[Figure 3, callout 16]

Each DP83867 PHY (GEM0 U198) controls two LEDs in the J307 two port connector bezel. The PHY signal LED0 drives the green LED, and LED1 drives the yellow LED. The LED2 signal is not used.

The LED functional description is listed in the following table.

Table 14: Ethernet PHY LED Functional Description

DP83867IS PHY Pin		Type	Description
Name	Number		
LED_2	45	S, I/O, PD	By default, this pin indicates receive or transmit activity. Additional functionality is configurable using LEDCR1[11:8] register bits.
LED_1	46	S, I/O, PD	By default, this pin indicates that 100BASE-T link is established. Additional functionality is configurable using LEDCR1[7:4] register bits.
LED_0	47	S, I/O, PD	By default, this pin indicates that link is established. Additional functionality is configurable using LEDCR1[3:0] register bits.

The LED functions can be repurposed with a LEDCR1 register write available via the PHY's management data interface, MDIO/MDC.

See the TI DP83867 RGMII PHY data sheet at the [Texas Instruments](#) website for component details.

The detailed ACAP connections for the feature described in this section are documented in the VPK180 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

PMC MIO[49] and LPD MIO[13,15:16,20]: Power Enable

[Figure 3, callout 20-28]

The VPK180 allows the Versal ACAP to control the power to the various power domains. This is an active-High signal. It is connected to the components that are controlled using an open-drain buffer, U268 (VCC_PSLP_EN) or U254 (see others in the following table). The output of the buffers are pulled up with a 4.7K resistor to aid in the default boot state being set properly. When J345 is installed, the Versal ACAP has control over this power enable. When not installed, the enable is controlled by UTIL_5V0_PGOOD, which is an output from the 5.0V power supply (U191). See schematic page 90 for more information (see [Jumpers](#) for defaults).

Table 15: PMC MIO[49] and LPD MIO[13,15:16,20] Power Domains

ACAP Pin	Signal	Power Domains
PMC MIO49	VCC_PSLP_EN	LPDMGTYAVCC, VCCO_502, VCC_PSLP_CPM5, LPDMGTYAVTT
LPD MIO 13	VCC_SOC_EN	VCC_SOC
LPD MIO 15	VCC_PSFP_EN	VCC_PSFP
LPD MIO 16	VCC1V1_LP4_AUX_EN	VCCAUX,VCC1V1_LP4
LPD MIO 20	VCC_PL_EN	VCCINT
LPD MIO 23	VADJ_FMC_EN	VADJ_FMC

Note: See [LPD MIO\[23\]: VADJ_FMC Power Rail](#) for more information.

LPD MIO[21:22] Fan PWM

The ACAP PS bank 502 MIO21 (MIO21_FAN_PWM_VERSAL) is connected to J347 pin 3. When J347 is selected as 2-3 (see [Jumpers](#) for defaults), the ACAP is able to control the fan PWM speed. A controller application must be created to drive this logic. The ACAP PS bank 502 MIO22 (MIO22_FAN_TACH_VERSAL) is connected J348 pin 3. This signal is fed by a 2N7002 MOSFET (Q46), which is in turn connected to the 12V fan tachometer feedback. The 2N7002 is a N-Channel 60 V MOSFET. For more details, see [Cooling Fan Connector](#).

LPD MIO[23]: VADJ_FMC Power Rail

The VPK180 evaluation board implements the ANSI/VITA 57.4 IPMI support functionality. The power control of the VADJ_FMC power rail is managed by the ZU4 U125 system controller. This rail powers FMCP HSPC J51 VADJ pins, as well as the XCVP1802 U1 VCCO on the FMCP interface banks 709 and 710. The valid values of the VADJ_FMC rail are 0, 1.2V, or 1.5V. At power on, the system controller detects if an FMC module is installed on J51. The Versal ACAP also has control over the active-High enable line on the voltage regulator.

If the Versal ACAP has enabled the voltage regulator (active-High), the following sequence of actions occur:

- If no card is attached to a FMCP connector, the VADJ_FMC voltage is set to 1.5V
- When an FMC card is attached, its IIC EEPROM is read to find a VADJ voltage supported by both the VPK180 board and the FMC module, within the available choices of 0, 1.0V, 1.2V, or 1.5V
- If no valid information is found, or no voltage range can be matched in an attached FMC card IIC EEPROM, the VADJ_FMC rail is set to 0.0V

The system controller user interface allows the FMC IPMI routine to be overridden and an explicit value can be set for the VADJ_FMC rail. The override mode is useful for FMC mezzanine cards that do not contain valid IPMI EPROM data defined by the ANSI/VITA 57.4 specification.

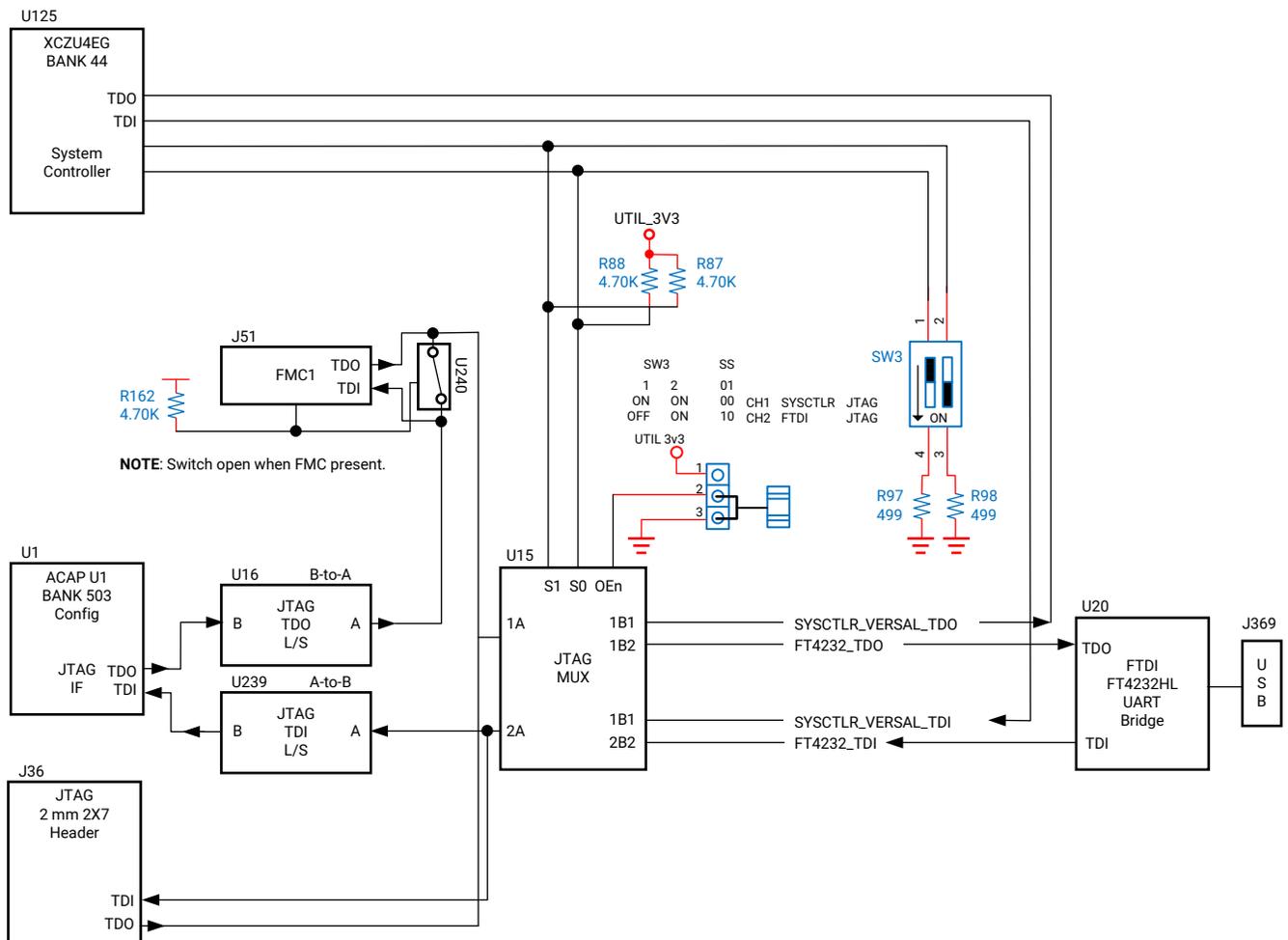
JTAG Chain

[Figure 3, callout 6, 9, Figure 4, callout 11, 13]

The JTAG chain includes:

- J36 2x7 2 mm shrouded, keyed JTAG pod flat cable connector
- J344 USB-A micro connector connected to U20 FT4232HL USB-JTAG bridge
- U125 XCZU4EG System Controller bank 44

Figure 17: JTAG Chain Block Diagram



X26554-110122

See [Versal ACAP Configuration](#) for information on JTAG programming via:

- FTDI FT4232 USB-to-JTAG/USB-UART device (U20) connected to USB 3.1 type-C connector (J369)
- JTAG pod flat cable connector J36 (2 mm 2x7 shrouded/keyed)

See the "FT4232HL UART Connections" figure in [PMC MIO\[42:43\] UART0](#) for an overview of FT4232 U20 JTAG and USB-UART connectivity.

Clock Generation

The VPK180 board provides fixed and variable clock sources for the XCVC1802 U1 ACAP and other function blocks. The following table lists the source devices for each clock.

Table 16: Clock Sources

Ref. Des.	Feature	Notes	Schematic Page
U248	DDR4 DIMM CLK, 200 MHz, 3.3V LVDS, 0x60	Skyworks/Silicon Labs 570BAB000299DG	3
U3	DDR4 DIMM CLK, 200 MHz, 3.3V LVDS, 0x60	Skyworks/Silicon Labs 570BAB000299DG	4
U4	DDR4 DIMM CLK, 200 MHz, 3.3V LVDS, 0x60	Skyworks/Silicon Labs 570BAB000299DG	5
U312	HSDP System Controller REFCLK1, 156.25 MHz, 3.3V LVDS	CTS 626L15625I3T	8
U313	HSDP System Controller REFCLK1, 156.25 MHz, 3.3V LVDS	CTS 626L15625I3T	8
U32	ACAP U1 REF CLK, 33.33 MHz, 1.8V CMOS, 0x5D	Skyworks/Silicon Labs 570JAC000900DGR	54
U298	ACAP U1 GTM CLK, 156.25 MHz, 1.8V LVDS, 0x09	Renesas RC21008A065GND	61
U299	ACAP U1 GTM CLK, 156.25 MHz, 1.8V LVDS, 0x09	Renesas RC21008A065GND	62
U219	IEEE-1588 eCPRI CLK, various, 3.3V, 0x5B	Renesas/IDT 8A34001E-000AJG8	90

The detailed ACAP connections for the feature described in this section are documented in the VPK180 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

Programmable LPDDR4 SI570 Clock

[[Figure 3](#), callout 38, 39, 40]

The VPK180 evaluation board has I2C programmable SI570 low-jitter 3.3V LVDS differential oscillators (U248, U3, U4) connected to the GC inputs of U1 DDR4 DIMM interface bank 702, 705, and 708, respectively. The LPDDR4_CLK1_P/N, LPDDR4_CLK2_P/N and LPDDR4_CLK3_P/N series capacitor coupled clock signals are connected to XCVP1802 ACAP U1. At power-up, this clock defaults to an output frequency of 200.000 MHz. User applications or the system controller can change the output frequency within the range of 10 MHz to 945 MHz through the I2C bus interface. Power cycling the VPK180 evaluation board reverts this user clock to the default frequency of 200.000 MHz.

- Programmable oscillator: Skyworks/Silicon Labs SI570BAB000299DG
- 10 MHz-945 MHz range, 200.000 MHz default

- I2C address 0x60
- LVDS differential output, total stability: 61.5 ppm

Programmable SI570 REF Clock

[Figure 3, callout 37]

The VPK180 evaluation board has an I2C programmable SI570 low-jitter 1.8V CMOS single-ended oscillator (U32). The 33.333 MHz REF_CLK clock signal is connected to XCVP1802 ACAP U1 configuration bank 503. At power-up, this clock defaults to an output frequency of 33.333333... MHz (33 + 1/3 MHz). User applications or the system controller can change the output frequency within the range of 10 MHz to 945 MHz through the I2C bus interface. Power cycling the VPK180 evaluation board reverts this user clock to the default frequency of 33.333333... MHz (33 + 1/3 MHz).

- Programmable oscillator: Skyworks/Silicon Labs SI570JAC000900DG
- 10 MHz-945 MHz range, 33.333 MHz default
- I2C address 0x5D
- CMOS single-ended output, total stability: 61.5 ppm

Programmable MGT RC21008A REF Clocks

[Figure 3, callout 34]

The VPK180 evaluation board has two I2C programmable RC21008A high-performance frequency synthesizers (U298, U299) that provide excellent phase jitter on reference clocks. The output has been configured as a 1.8V LVDS output. The 156.25 MHz RC21008A_GTCLK[1:2]_OUT[0:7] clock signals are connected to the XCVP1802 ACAP U1 transceiver banks. See the table in the [Transceivers](#) section for connectivity. See schematic pages 61/62 for further details.

At power-up, this clock defaults to an output frequency of 156.25 MHz. User applications or the system controller can change the output frequency within the range of 0.001 MHz to 650 MHz through the I2C bus interface. Power cycling the VPK180 evaluation board reverts this user clock to the default frequency of 156.25 MHz.

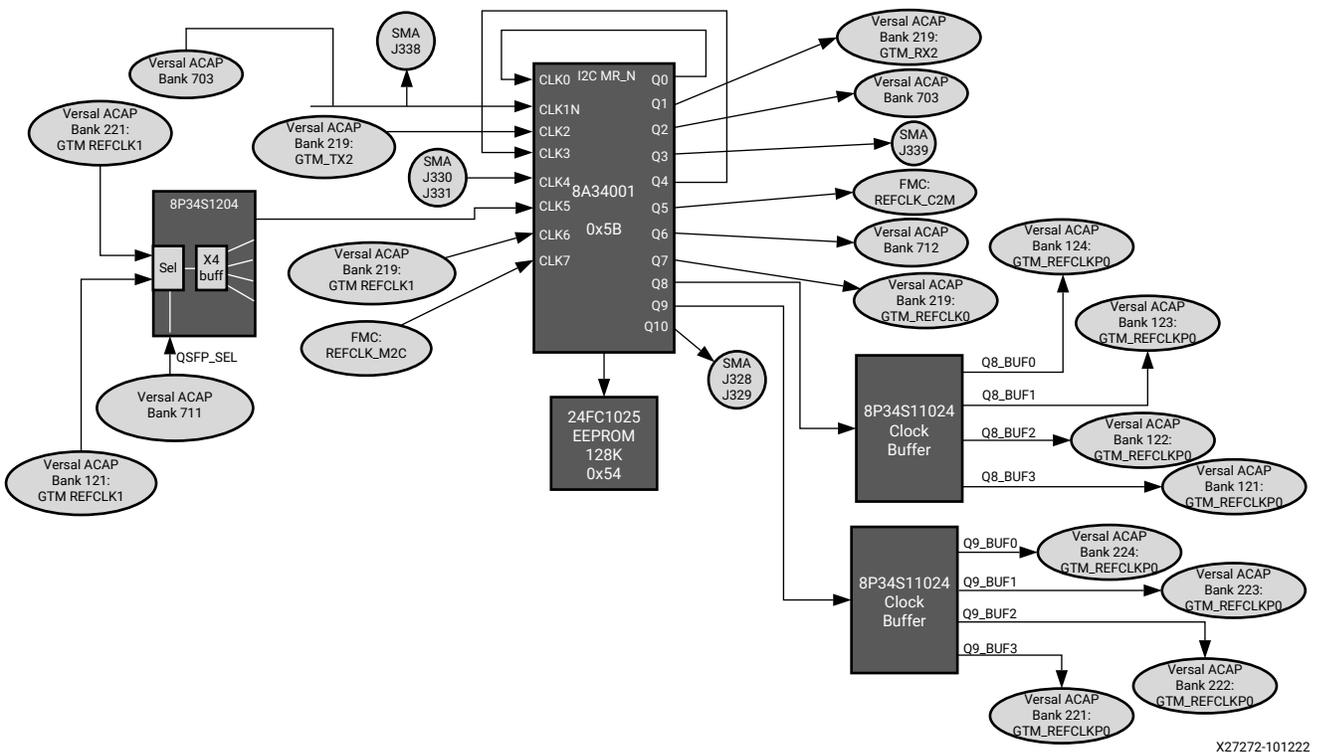
- Programmable frequency synthesizer: Renesas RC21008A065#BBO
- 0.001 MHz-650 MHz range, 156.25 MHz default
- I2C address 0x09
- LVDS differential output

IEEE-1588 eCPRI Programmable Synchronization Management Unit

[Figure 3, callout 46]

The 8A34001 synchronization management unit (SMU) provides tools to manage timing references, clock sources, and timing paths for IEEE 1588 and Synchronous Ethernet (SyncE) based clocks. The PLL channels can act independently as frequency synthesizers, jitter attenuators, digitally controlled oscillators (DCO), or digital phase lock loops (DPLL). The following block diagram can aid in quickly determining the overall clock tree for the 8A34001 (U219). See schematic pages 90-91 for details. For more details on programming and controlling the 8A34001, see the [Renesas/Integrated Device Technology, Inc. \(IDT\)](https://www.renesas.com/en/integrated-device-technology) website and data sheet.

Figure 18: IEEE-1588 eCPRI Block Diagram



X27272-101222

Transceivers

The Versal ACAP has 168 PL transceivers including 28 GTYP and 140 GTM type transceivers.

The following table contains the mapping to hardened features, quads, channel locations, as well as general features.

Table 17: Transceiver Mapping

VPK180 XCVP1802 LSV4072 GTY/GTM Mapping								
[UNUSED]	ch3	GTM Quad 124 X0Y22 BQ [RN]	DCMAC X0Y6		ILKN X0Y2	GTM Quad 224 X1Y22 CY [LN]	ch3	[UNUSED]
QSFDD_5 Lane 8	ch2						ch2	QSFDD_6 Lane 8
[UNUSED]	ch1						ch1	[UNUSED]
QSFDD_5 Lane 7	ch0						ch0	QSFDD_6 Lane 7
[UNUSED]	refclk1						refclk1	[UNUSED]
8A34001 Q8 BUF0	refclk0						refclk0	8A34001 Q9 BUF0
[UNUSED]	ch3	GTM Quad 123 X0Y21 BP [RN]				GTM Quad 223 X1Y21 CX [LN]	ch3	[UNUSED]
QSFDD_5 Lane 6	ch2						ch2	QSFDD_6 Lane 6
[UNUSED]	ch1						ch1	[UNUSED]
QSFDD_5 Lane 5	ch0						ch0	QSFDD_6 Lane 5
[UNUSED]	refclk1						refclk1	[UNUSED]
8A34001 Q8 BUF1	refclk0						refclk0	8A34001 Q9 BUF1
[UNUSED]	ch3	GTM Quad 122 X0Y20 BO [RN] (RCAL)	MRMAC X0Y7		DCMAC X1Y5	GTM Quad 222 X1Y20 CW [LN]	ch3	[UNUSED]
QSFDD_5 Lane 4	ch2						ch2	QSFDD_6 Lane 4
[UNUSED]	ch1						ch1	[UNUSED]
QSFDD_5 Lane 3	ch0						ch0	QSFDD_6 Lane 3
[UNUSED]	refclk1						refclk1	[UNUSED]
8A34001 Q8 BUF2	refclk0						refclk0	8A34001 Q9 BUF2
[UNUSED]	ch3	GTM Quad 121 X0Y19 BN [RN]	MRMAC X0Y6			GTM Quad 221 X1Y19 CV [LN]	ch3	[UNUSED]
QSFDD_5 Lane 2	ch2						ch2	QSFDD_6 Lane 2
[UNUSED]	ch1						ch1	[UNUSED]
QSFDD_5 Lane 1	ch0						ch0	QSFDD_6 Lane 1
8A34001 CLK5 IN MUX1	refclk1						refclk1	8A34001 CLK5 IN MUX0
8A34001 Q8 BUF3	refclk0						refclk0	8A34001 Q9 BUF3

Table 17: Transceiver Mapping (cont'd)

VPK180 XCVP1802 LSVC4072 GTY/GTM Mapping									
						HSC X0Y3	GTM Quad 220 X1Y18 CU [LN] (RCAL)	ch3	[UNUSED]
								ch2	[UNUSED]
								ch1	[UNUSED]
								ch0	[UNUSED]
								refclk1	[UNUSED]
								refclk0	[UNUSED]
							GTM Quad 219 X1Y17 CT [LN]	ch3	GTM_219 SMAs TX/RX
								ch2	8A34001 1PPS Clocks CLK2 IN / Q1 OUT
								ch1	[UNUSED]
								ch0	[UNUSED]
								refclk1	8A34001 CLK6 IN
								refclk0	8A34001 Q7 OUT
SLR Crossing									
QSPDD_4 Lane 8	ch3	GTM Quad 118 X0Y16 BM [RUC]	DCMAC X0Y4		ILKN X0Y1	GTM Quad 218 X1Y16 CS [LUC]	ch3	[UNUSED]	
QSPDD_4 Lane 7	ch2			ch2			[UNUSED]		
QSPDD_4 Lane 6	ch1			ch1			[UNUSED]		
QSPDD_4 Lane 5	ch0			ch0			[UNUSED]		
[UNUSED]	refclk1			refclk1			[UNUSED]		
RC21008A_GTCLK2_ OUT7	refclk0			refclk0			[UNUSED]		
QSPDD_4 Lane 4	ch3	GTM Quad 117 X0Y15 BL [RUC]				GTM Quad 217 X1Y15 CR [LUC]	ch3	[UNUSED]	
QSPDD_4 Lane 3	ch2			ch2			OSFP Lane 8		
QSPDD_4 Lane 2	ch1			ch1			[UNUSED]		
QSPDD_4 Lane 1	ch0			ch0			OSFP Lane 7		
[UNUSED]	refclk1			refclk1			[UNUSED]		
RC21008A_GTCLK2_ OUT6	refclk0			refclk0			RC21008A_GTCLK1_ OUT7		

Table 17: Transceiver Mapping (cont'd)

VPK180 XCVP1802 LSVC4072 GTY/GTM Mapping								
[UNUSED]	ch3	GTM Quad 116 X0Y14 BK [RUC] (RCAL)	MRMAC X0Y5		DCMAC X1Y3	GTM Quad 216 X1Y14 CQ [LUC]	ch3	OSFP Lane 6
SFPDD_4 Lane 2	ch2						ch2	[UNUSED]
[UNUSED]	ch1						ch1	OSFP Lane 5
SFPDD_4 Lane 1	ch0						ch0	[UNUSED]
[UNUSED]	refclk1						refclk1	[UNUSED]
RC21008A_GTCLK2_OUT5	refclk0						refclk0	RC21008A_GTCLK1_OUT6
[UNUSED]	ch3	GTM Quad 115 X0Y13 BJ [RUC]	MRMAC X0Y4			GTM Quad 215 X1Y13 CP [LUC]	ch3	[UNUSED]
SFPDD_3 Lane 2	ch2						ch2	OSFP Lane 4
[UNUSED]	ch1						ch1	OSFP Lane 3
SFPDD_3 Lane 1	ch0						ch0	[UNUSED]
[UNUSED]	refclk1						refclk1	[UNUSED]
RC21008A_GTCLK2_OUT4	refclk0						refclk0	RC21008A_GTCLK1_OUT5
					HSC X0Y2	GTM Quad 214 X1Y12 CO [LUC] (RCAL)	ch3	[UNUSED]
							ch2	OSFP Lane 2
							ch1	[UNUSED]
							ch0	OSFP Lane 1
							refclk1	[UNUSED]
							refclk0	RC21008A_GTCLK1_OUT4
						GTM Quad 213 X1Y11 CN [LUC]	ch3	[UNUSED]
							ch2	[UNUSED]
							ch1	[UNUSED]
							ch0	[UNUSED]
							refclk1	[UNUSED]
							refclk0	[UNUSED]
SLR Crossing								

Table 17: Transceiver Mapping (cont'd)

VPK180 XCVP1802 LSV4072 GTY/GTM Mapping								
QSFDD_3 Lane 8	ch3	GTM Quad 112 X0Y10 BI [RC]	DCMAC X0Y2		ILKN X0Y0	GTM Quad 212 X1Y10 CM [LC]	ch3	[UNUSED]
QSFDD_3 Lane 7	ch2						ch2	[UNUSED]
QSFDD_3 Lane 6	ch1						ch1	[UNUSED]
QSFDD_3 Lane 5	ch0						ch0	[UNUSED]
GTM_REFCLK_112 SMAs	refclk1						refclk1	[UNUSED]
RC21008A_GTCLK2_OUT3	refclk0						refclk0	[UNUSED]
QSFDD_3 Lane 4	ch3	GTM Quad 111 X0Y9 BH [RC]				GTM Quad 211 X1Y9 CL [LC]	ch3	QSFDD_1 Lane 8
QSFDD_3 Lane 3	ch2						ch2	QSFDD_2 Lane 8
QSFDD_3 Lane 2	ch1						ch1	QSFDD_2 Lane 7
QSFDD_3 Lane 1	ch0						ch0	QSFDD_1 Lane 7
GTM_REFCLK_111 SMAs	refclk1						refclk1	[UNUSED]
RC21008A_GTCLK2_OUT2	refclk0						refclk0	RC21008A_GTCLK1_OUT3
[UNUSED]	ch3	GTM Quad 110 X0Y8 BG [RC] (RCAL)	MRMAC X0Y3		DCMAC X1Y1	GTM Quad 210 X1Y8 CK [LC]	ch3	QSFDD_1 Lane 6
SFPDD_2 Lane 2	ch2						ch2	QSFDD_2 Lane 6
[UNUSED]	ch1						ch1	QSFDD_2 Lane 5
SFPDD_2 Lane 1	ch0						ch0	QSFDD_1 Lane 5
GTM_REFCLK_110 SMAs	refclk1						refclk1	[UNUSED]
RC21008A_GTCLK2_OUT1	refclk0						refclk0	RC21008A_GTCLK1_OUT2
[UNUSED]	ch3	GTM Quad 109 X0Y7 BF [RC]	MRMAC X0Y2			GTM Quad 209 X1Y7 CJ [LC]	ch3	QSFDD_2 Lane 4
SFPDD_1 Lane 2	ch2						ch2	QSFDD_1 Lane 4
[UNUSED]	ch1						ch1	QSFDD_2 Lane 3
SFPDD_1 Lane 1	ch0						ch0	QSFDD_1 Lane 3
GTM_REFCLK_109 SMAs	refclk1						refclk1	[UNUSED]
RC21008A_GTCLK2_OUT0	refclk0						refclk0	RC21008A_GTCLK1_OUT1

Table 17: Transceiver Mapping (cont'd)

VPK180 XCVP1802 LSVC4072 GTY/GTM Mapping								
					HSC X0Y1	GTM Quad 208 X1Y6 CI [LC] (RCAL)	ch3	QSFDD_1 Lane 2
							ch2	QSFDD_2 Lane 2
							ch1	QSFDD_1 Lane 1
							ch0	QSFDD_2 Lane 1
							refclk1	[UNUSED]
							refclk0	RC21008A_GTCLK1_OUT0
						GTM Quad 207 X1Y5 CH [LC]	ch3	[UNUSED]
							ch2	[UNUSED]
							ch1	[UNUSED]
							ch0	[UNUSED]
							refclk1	[UNUSED]
							refclk0	[UNUSED]
SLR Crossing								
[UNUSED]	ch3	GTYP Quad 106 X0Y6 BE [RLC] (RCAL)	PCIe X0Y1		MRMAC X1Y1	GTM Quad 206 X1Y4 CG [LLC]	ch3	[UNUSED]
[UNUSED]	ch2			ch2			[UNUSED]	
[UNUSED]	ch1			ch1			[UNUSED]	
[UNUSED]	ch0			ch0			[UNUSED]	
[UNUSED]	refclk1			refclk1			[UNUSED]	
[UNUSED]	refclk0			refclk0			[UNUSED]	

Table 17: Transceiver Mapping (cont'd)

VPK180 XCVP1802 LSV4072 GTY/GTM Mapping									
[UNUSED]	ch3	GTYP (CPM5) Quad 105 X0Y5 BD [RS] (RCAL)	CPM5		DCMAC X1Y0	GTM Quad 205 X1Y3 CF [LLC]	ch3	[UNUSED]	
[UNUSED]	ch2						ch2	[UNUSED]	
[UNUSED]	ch1						ch1	[UNUSED]	
[UNUSED]	ch0						ch0	[UNUSED]	
[UNUSED]	refclk1						refclk1	[UNUSED]	
[UNUSED]	refclk0						refclk0	[UNUSED]	
[UNUSED]	ch3	GTYP (CPM5) Quad 104 X0Y4 BC [RS]				GTM Quad 204 X1Y2 CE [LLC]	ch3	[UNUSED]	
[UNUSED]	ch2						ch2	[UNUSED]	
[UNUSED]	ch1						ch1	[UNUSED]	
HSDP_VERSAL_SYSC TL GTH Lane 0	ch0						ch0	[UNUSED]	
[UNUSED]	refclk1						refclk1	[UNUSED]	
HSDP_VERSAL_156_25_REFCLK2	refclk0						refclk0	[UNUSED]	
[UNUSED]	ch3	GTYP (CPM5) Quad 103 X0Y3 BB [RS]				HSC X0Y0	GTM Quad 203 X1Y1 CD [LLC] (RCAL)	ch3	[UNUSED]
[UNUSED]	ch2							ch2	[UNUSED]
[UNUSED]	ch1							ch1	[UNUSED]
[UNUSED]	ch0							ch0	[UNUSED]
[UNUSED]	refclk1							refclk1	[UNUSED]
[UNUSED]	refclk0							refclk0	[UNUSED]
[UNUSED]	ch3	GTYP (CPM5) Quad 102 X0Y2 BA [RS]					GTM Quad 202 X1Y0 CC [LLC]	ch3	[UNUSED]
[UNUSED]	ch2							ch2	[UNUSED]
[UNUSED]	ch1							ch1	[UNUSED]
HSDP_VERSAL USB Type-C Lane 2	ch0							ch0	[UNUSED]
[UNUSED]	refclk1							refclk1	[UNUSED]
HSDP_VERSAL_156_25_REFCLK1	refclk0							refclk0	[UNUSED]
						MRMAC X1Y0	GTYP Quad 201 X1Y1 CB [LS] (RCAL)	ch3	FMC DP7
								ch2	FMC DP6
								ch1	FMC DP5
								ch0	FMC DP4
								refclk1	[UNUSED]
								refclk0	FMCP1_GBCLK1

Table 17: Transceiver Mapping (cont'd)

VPK180 XCVP1802 LSV4072 GTY/GTM Mapping									
						PCIe X1Y0	GTYP Quad 200 X1Y0 CA [LS]	ch3	FMC DP3
								ch2	FMC DP2
								ch1	FMC DP1
								ch0	FMC DP0
								refclk1	[UNUSED]
								refclk0	FMCP1_GBCLK0

GTYP Transceivers

[Figure 3, callout 1]

The ACAP (U1) bank 200 and bank 201 GTYP transceivers are wired to the FMCP connector (J51). See schematic pages 9 and 46 for details.

The GTY/GTYP transceivers in the Versal architecture are power-efficient transceivers, supporting line rates from 1.25 Gb/s to 32.75 Gb/s. The GTY/GTYP transceivers are highly configurable and tightly integrated with the programmable logic resources of the Versal architecture. For more information, see the *Versal ACAP GTY and GTYP Transceivers Architecture Manual* (AM002).

GTYP102/104: High-speed Debug Port Connectivity

[Figure 3, callout 9]

See the *Versal Architecture and Product Data Sheet: Overview* (DS950) for more information about the high-speed debug port (HSDP) feature.

See schematic pages 8 and 36, as well as the [VPK180 Evaluation Board](#) website for more details on connectivity. See schematic page 8 for details on the clocking configuration.

GTYP200/201: FPGA Mezzanine Card Interface

[Figure 3, callout 17]

The detailed ACAP connections for the feature described in this section are documented in the VPK180 board XDC file, referenced in [Appendix B: Xilinx Design Constraints](#).

FMC+ Connector Type

The Samtec SEAF series 1.27 mm (0.050 in) pitch mates with the SEAM series connector. For more information about the SEAF series connectors, see the [Samtec, Inc.](#) website. The 560-pin FMC+ connector defined by the FMC specification (see [Appendix A: VITA 57.4 FMCP Connector Pinouts](#)) provides connectivity for up to:

- 160 single-ended or 80 differential user-defined signals
- 24 transceiver differential pairs
- 6 transceiver (GBTCLK) differential clocks
- 4 differential (CLK) clocks
- 1 differential (REFCLK) clock (both C2M and M2C pairs)
- 1 differential (SYNC) clock (both C2M and M2C pairs)
- 239 ground and 17 power connections

For more information about the VITA 57.4 FMC+ specification, see the [VITA FMC Marketing Alliance](#) website.

GTM Transceivers

[[Figure 3](#), callout 1]

The GTM transceiver in the Versal Premium Series is a high-performance transceiver, supporting a maximum line rate 112.0 Gb/s PAM4. The GTM transceiver is a tightly integrated programmable logic resource of the ACAP and the integrated networking IP, such as the DCMAC or MRMAC.

For each of the interfaces described in the following sections, see the table in the [Transceivers](#) section. This table depicts the mapping from quads, channels, to lanes, along with associated hardened IP and associated clocks.

GTM109/110/115/116: SFPDD1/2/3/4

[[Figure 3](#), callout 15]

- The ACAP (U1) bank 109 GTM transceivers are wired to the SFPDD1 connector J350.
- The ACAP (U1) bank 110 GTM transceivers are wired to the SFPDD2 connector J352.
- The ACAP (U1) bank 115 GTM transceivers are wired to the SFPDD3 connector J385.
- The ACAP (U1) bank 116 GTM transceivers are wired to the SFPDD4 connector J351.

The connector is a Molex connector 2047301000, rated at 56 Gb/s per lane. The evaluation board has been optimized for 56 Gb/s per lane to provide 100GAUI-1 functionality.

For connectivity details, see the table in the [Transceivers](#) section and schematic pages 63/64. See the *Versal ACAP GTM Transceivers Architecture Manual* ([AM017](#)) for more details on 112 Gb/s GTM-Quad configurations.

GTM208/209/210/211: QSFPDD1/2

[[Figure 3](#), upper callout 14]

The ACAP (U1) banks 208/209/210/211 GTM transceivers are split and wired to the QSFPDD1 connector J1 and QSFPDD2 connector J2. The connectors are Molex connector 2147334000 rated at 112 Gb/s per lane.

The transceivers are wired in an optimized pattern to allow the QSFPDD1 connector to be operated at 112 Gb/s per lane and QSFPDD2 can be operated at 56 Gb/s per lane. This configuration was chosen to provide 800GAUI-8 functionality. However, while QSFPDD1 is operating at 800 Gb/s modes, QSFPDD2 cannot be used. To use QSFPDD2, QSFPDD1 is limited to 56 Gb/s. This allows for both connectors to be operated simultaneously at 400GAUI-8 or similar modes.

For connectivity details, see the table in the [Transceivers](#) section and schematic page 57. See the *Versal ACAP GTM Transceivers Architecture Manual (AM017)* for more details on 112 Gb/s GTM-Quad configurations.

GTM111/112/117/118: QSFPDD3/4

[[Figure 3](#), bottom and lower left callout 14]

The ACAP (U1) banks 111/112 GTM transceivers are wired to the QSFPDD3 connector J355. The ACAP (U1) banks 117/118 GTM transceivers are wired to the QSFPDD4 connector J354. The connectors are Molex connector 2147334000, rated at 112 Gb/s per lane.

The transceivers are wired in an optimized pattern to be operated at 56 Gb/s per lane. This configuration was chosen to provide 400GAUI-8 functionality.

For connectivity details, see the table in the [Transceivers](#) section and schematic page 58. See the *Versal ACAP GTM Transceivers Architecture Manual (AM017)* for more details on GTM-Quad configurations.

GTM121/122/123/124/221/222/223/224: QSFPDD5/6

[[Figure 3](#), left callout 14]

The ACAP (U1) banks 121/122/123/124 GTM transceivers are wired to the QSFPDD5 connector J359. The ACAP (U1) banks 221/222/223/224 GTM transceivers are wired to the QSFPDD6 connector J358. The connectors are Molex connector 2147334000, rated at 112 Gb/s per lane.

The transceivers are wired in an optimized pattern to be operated at 112 Gb/s per lane. This configuration was chosen to provide 800GAUI-8 functionality.

For connectivity details, see the table in the [Transceivers](#) section and schematic page 59. See the *Versal ACAP GTM Transceivers Architecture Manual (AM017)* for more details on GTM-Quad configurations.

GTM214/215/216/217: OSFP

[Figure 3, callout 55]

The ACAP (U1) banks 214/215/216/217 GTM transceivers are wired to the QSFPDD6 connector J362. The connector is TE connectivity connector 2344064-4, rated at 112 Gb/s per lane.

The transceivers are wired in an optimized pattern to be operated at 112 Gb/s per lane. This configuration was chosen to provide 800GAUI-8 functionality.

For connectivity details, see the table in the [Transceivers](#) section and schematic page 60. See the *Versal ACAP GTM Transceivers Architecture Manual (AM017)* for more details on GTM-Quad configurations.

GTM219: SMA/1588 PPS

[Figure 3, callout 41]

The ACAP (U1) bank 219 GTM transceivers are wired to the SMA connectors J373, J374, J375, and J376. The connectors are the Carlisle SMA TMB-V5F2-3L1, rated at 34 GHz. The remainder of the ACAP (U1) bank 219 GTM transceivers are wired to the Renesas 8A34001 system synchronizer (U219). This provides for an IEEE 1588 PPS signal. This is intended to be coupled with REFCLK0, which has been tied to an output from the Renesas 8A34001 (U219) system synchronizer for IEEE 1588 use.

The transceivers are wired in an optimized pattern to be operated at 112 Gb/s per lane. This configuration was chosen to provide flexibility for evaluation of GTM transceivers.

For connectivity details, see the table in the [Transceivers](#) section and schematic page 18. See the *Versal ACAP GTM Transceivers Architecture Manual (AM017)* for more details on GTM-Quad configurations.

QSFP-DD Control Signals

The QSFP-DD control signals can be asserted in multiple ways. Each QSFP-DD has an I2C connection to the I2C1 bus through the I2C multiplexer (TCA9548PWR U35) as shown in the [PMC MIO\[44:45\] I2C1 Bus](#) section.

The following table lists the transceiver module control signals.

Table 18: Transceiver Module Control Signals

Signal Name	Feature	Notes	Schematic Page
QSFPDD_I2C_SDA	Two-wire interface data	U35 I2C MUX	56-59
QSFPDD_I2C_SCL	Two-wire interface clock	U35 I2C MUX	56-59

Table 18: Transceiver Module Control Signals (cont'd)

Signal Name	Feature	Notes	Schematic Page
QSFDD1_MODSELL	Module select	U233 P00	6, 55, 57
QSFDD1_RESETL	Module reset	U1 Bank 711	6, 57
QSFDD1_MODPRSL	Module present	U1 Bank 711	6, 57
QSFDD1_INTL	Interrupt	U1 Bank 711	6, 57
QSFDD1_INITMODE	Low power mode	U1 Bank 711	6, 57
QSFDD2_MODSELL	Module select	U233 P01	6, 55, 57
QSFDD2_RESETL	Module reset	U1 Bank 711	6, 57
QSFDD2_MODPRSL	Module present	U1 Bank 711	6, 57
QSFDD2_INTL	Interrupt	U1 Bank 711	6, 57
QSFDD2_INITMODE	Low power mode	U1 Bank 711	6, 57
QSFDD3_MODSELL	Module select	U233 P02	6, 55, 58
QSFDD3_RESETL	Module reset	U1 Bank 711	6, 58
QSFDD3_MODPRSL	Module present	U1 Bank 711	6, 58
QSFDD3_INTL	Interrupt	U1 Bank 711	6, 58
QSFDD3_INITMODE	Low power mode	U1 Bank 711	6, 58
QSFDD4_MODSELL	Module select	U233 P03	6, 55, 58
QSFDD4_RESETL	Module reset	U1 Bank 711	6, 58
QSFDD4_MODPRSL	Module present	U1 Bank 711	6, 58
QSFDD4_INTL	Interrupt	U1 Bank 711	6, 58
QSFDD4_INITMODE	Low power mode	U1 Bank 711	6, 58
QSFDD5_MODSELL	Module select	U233 P05	6, 55, 59
QSFDD5_RESETL	Module reset	U1 Bank 711	6, 59
QSFDD5_MODPRSL	Module present	U1 Bank 711	6, 59
QSFDD5_INTL	Interrupt	U1 Bank 711	6, 59
QSFDD5_INITMODE	Low power mode	U1 Bank 711	6, 59
QSFDD6_MODSELL	Module select	U233 P06	6, 55, 59
QSFDD6_RESETL	Module reset	U1 Bank 711	6, 59
QSFDD6_MODPRSL	Module present	U1 Bank 711	6, 59
QSFDD6_INTL	Interrupt	U1 Bank 711	6, 59
QSFDD6_INITMODE	Low power mode	U1 Bank 711	6, 59
OSFP_I2C_SDA	Two-wire interface data	U35 I2C MUX	56, 60
OSFP_I2C_SCL	Two-wire interface clock	U35 I2C MUX	56, 60
OSFP_H_LPWN_N	U1 to module low power mode	U2 level shift	7, 57, 60
OSFP_H_PRN_N	Module to U1 module present	U9 level shift	7, 57, 60
OSFP_H_INTN	Module to U1 interrupt	U9 level shift	7, 57, 60
OSFP_H_RSTN	U1 to module reset	U2 level shift	7, 57, 60
SFPDD1_I2C_SDA	Two-wire interface data	U322 I2C MUX	56, 63
SFPDD1_I2C_SCL	Two-wire interface clock	U322 I2C MUX	56, 63

Table 18: Transceiver Module Control Signals (cont'd)

Signal Name	Feature	Notes	Schematic Page
SFPDD1_CH0_TXFAULT	Module to U1 - fault condition detected	U1 Bank 709	6, 63
SFPDD1_CH0_TXDISABLE	U1 to module - transmitter disable	U1 Bank 709	6, 63
SFPDD1_CH0_SPEED1	Module receive rate selection	Float on board	63
SFPDD1_CH0_SPEED2	Module receive rate selection	Float on board	63
SFPDD1_CH0_RXLOS	Module to U1 - RX signal loss	U1 Bank 709	6, 63
SFPDD1_CH1_TXFAULTDD	U1 to module - transmitter disable	U1 Bank 709	6, 63
SFPDD1_CH1_TXDISABLEDD	Module to U1 - fault condition interrupt/detected	U1 Bank 709	6, 63
SFPDD1_CH1_SPEED1DD	Module receive - rate selection	Float on board	63
SFPDD1_CH1_SPEED2DD	Module receive - rate selection	Float on board	63
SFPDD1_CH1_RXLOSDD	Module to U1 - RX signal loss	U1 Bank 709	6, 63
SFPDD1_MOD_ABS	Module to U1 - module absent	U1 Bank 709	6, 63
SFPDD1_LPMODE	U1 to module - low power mode	Float on board	63
SFPDD1_RESETL	U1 to module - complete module reset	U1 Bank 709	6, 63
SFPDD2_I2C_SDA	Two-wire interface data	U322 I2C MUX	56, 63
SFPDD2_I2C_SCL	Two-wire interface clock	U322 I2C MUX	56, 63
SFPDD2_CH0_TXFAULT	Module to U1 - fault condition detected	U1 Bank 709	6, 63
SFPDD2_CH0_TXDISABLE	U1 to module - transmitter disable	U1 Bank 709	6, 63
SFPDD2_CH0_SPEED1	Module receive rate selection	Float on board	63
SFPDD2_CH0_SPEED2	Module receive rate selection	Float on board	63
SFPDD2_CH0_RXLOS	Module to U1 - RX signal loss	U1 Bank 709	6, 63
SFPDD2_CH1_TXFAULTDD	U1 to module - transmitter disable	U1 Bank 709	6, 63
SFPDD2_CH1_TXDISABLEDD	Module to U1 - fault condition interrupt/detected	U1 Bank 709	6, 63
SFPDD2_CH1_SPEED1DD	Module receive - rate selection	Float on board	63
SFPDD2_CH1_SPEED2DD	Module receive - rate selection	Float on board	63
SFPDD2_CH1_RXLOSDD	Module to U1 - RX signal loss	U1 Bank 709	6, 63
SFPDD2_MOD_ABS	Module to U1 - module absent	U1 Bank 709	6, 63
SFPDD2_LPMODE	U1 to module - low power mode	Float on board	63
SFPDD2_RESETL	U1 to module - complete module reset	U1 Bank 709	6, 63
SFPDD3_I2C_SDA	Two-wire interface data	U322 I2C MUX	56, 64
SFPDD3_I2C_SCL	Two-wire interface clock	U322 I2C MUX	56, 64
SFPDD3_CH0_TXFAULT	Module to U1 - fault condition detected	U1 Bank 710	6, 64
SFPDD3_CH0_TXDISABLE	U1 to module - transmitter disable	U1 Bank 710	6, 64
SFPDD3_CH0_SPEED1	Module receive - rate selection	Float on board	64
SFPDD3_CH0_SPEED2	Module receive - rate selection	Float on board	64
SFPDD3_CH0_RXLOS	Module to U1 - RX signal loss	U1 Bank 710	6, 64

Table 18: Transceiver Module Control Signals (cont'd)

Signal Name	Feature	Notes	Schematic Page
SFPDD3_CH1_TXFAULTDD	U1 to module - transmitter disable	U1 Bank 710	6, 64
SFPDD3_CH1_TXDISABLEDD	Module to U1 - fault condition interrupt/detected	U1 Bank 710	6, 64
SFPDD3_CH1_SPEED1DD	Module receive - rate selection	Float on board	64
SFPDD3_CH1_SPEED2DD	Module receive - rate selection	Float on board	64
SFPDD3_CH1_RXLOSDD	Module to U1 - RX signal loss	U1 Bank 710	6, 64
SFPDD3_MOD_ABS	Module to U1 - module absent	U1 Bank 710	6, 64
SFPDD3_LPMODE	U1 to module - low power mode	Float on board	64
SFPDD3_RESETL	U1 to module - complete module reset	U1 Bank 710	6, 64
SFPDD4_I2C_SDA	Two-wire interface data	U322 I2C MUX	56, 64
SFPDD4_I2C_SCL	Two-wire interface clock	U322 I2C MUX	56, 64
SFPDD4_CH0_TXFAULT	Module to U1 - fault condition detected	U1 Bank 710	6, 64
SFPDD4_CH0_TXDISABLE	U1 to module - transmitter disable	U1 Bank 710	6, 64
SFPDD4_CH0_SPEED1	Module receive rate selection	Float on board	64
SFPDD4_CH0_SPEED2	Module receive rate selection	Float on board	64
SFPDD4_CH0_RXLOS	Module to U1 - RX signal loss	U1 Bank 710	6, 64
SFPDD4_CH1_TXFAULTDD	U1 to module - transmitter disable	U1 Bank 710	6, 64
SFPDD4_CH1_TXDISABLEDD	Module to U1 - fault condition interrupt/detected	U1 Bank 710	6, 64
SFPDD4_CH1_SPEED1DD	Module receive - rate selection	Float on board	64
SFPDD4_CH1_SPEED2DD	Module receive - rate selection	Float on board	64
SFPDD4_CH1_RXLOSDD	Module to U1 - RX signal loss	U1 Bank 710	6, 64
SFPDD4_MOD_ABS	Module to U1 - module absent	U1 Bank 710	6, 64
SFPDD4_LPMODE	U1 to module - low power mode	Float on board	64
SFPDD4_RESETL	U1 to module - complete module reset	U1 Bank 710	6, 64

High-speed Debug Port

The PS includes an integrated Aurora 64B/66B block that is dedicated for accessing the debug packet controller (DPC) via a high-speed GT-based interface. This protocol to access the DPC is the high-speed debug port (HSDP) protocol. The HSDP provides bidirectional access to the device from an external host debug/trace module, allowing for high-speed debug and trace operations. The SmartLynq+ module can be connected to the Aurora interface to access the HSDP in the Versal ACAP. For more information, see the *SmartLynq+ Module User Guide* (UG1514). For information on the HSDP quad availability, see the *Versal ACAP Technical Reference Manual* (AM011).

Note: The VPK180 evaluation board has additional HSDP lanes provided for future System Controller use.

Note: The integrated HSDP Aurora interface is not available in all Versal ACAPs, which might support HSDP using a soft Aurora solution. This interface requires additional configuration in the Control, Interfaces, and Processing (CIPS) IP, a PL aurora implementation, and the use of additional gigabit transceivers.

User I/O

[Figure 4, callout 14, 15 and Figure 3, callout 44]

See [Switches](#) for default values.

The following table lists the net names, reference designators, and schematic pages for the user I/O.

Table 19: User I/O

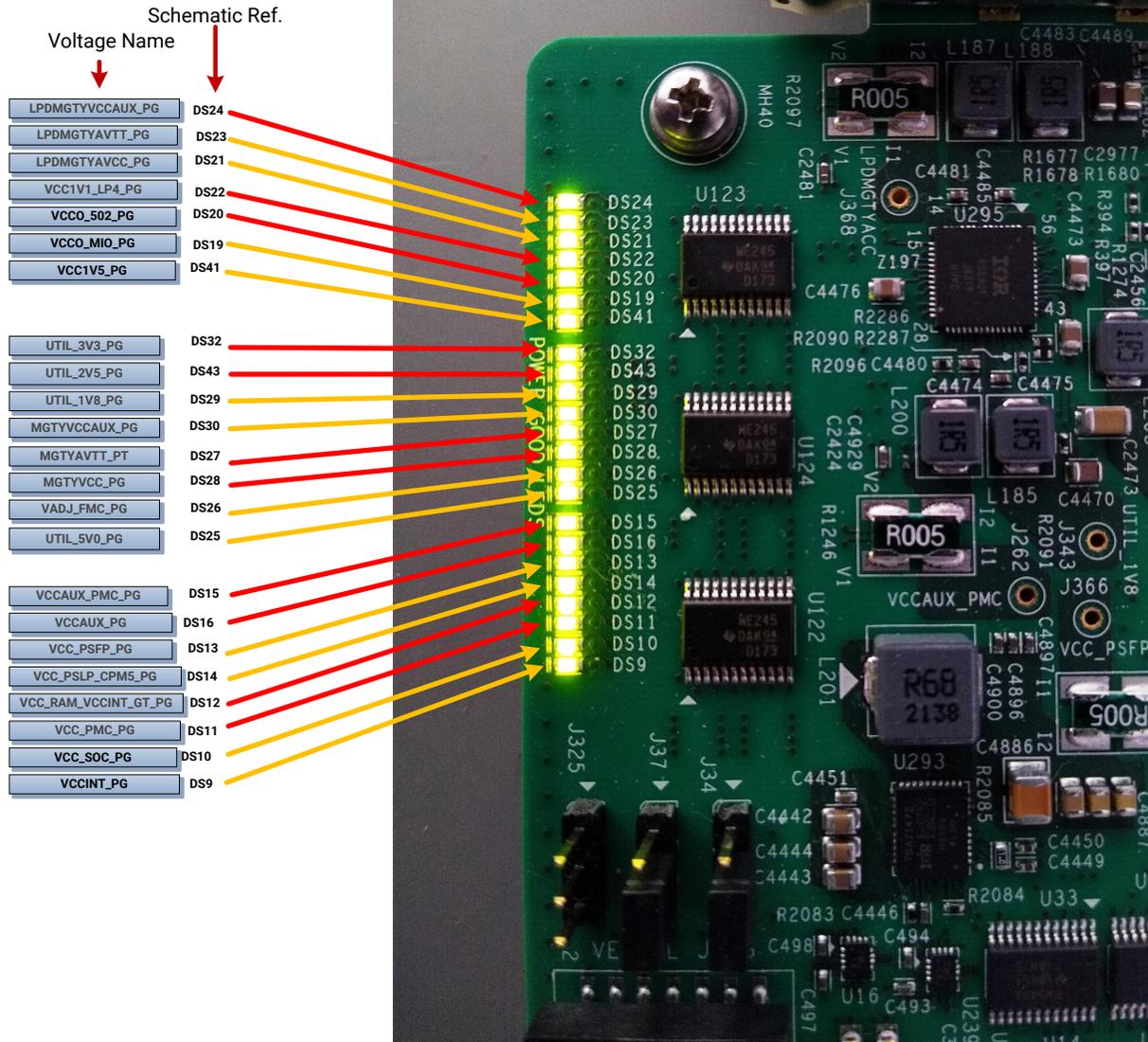
Net Name	Ref. Designator	Schematic Pages
GPIO_PB0	SW4	6/65
GPIO_PB1	SW5	6/65
GPIO_DIP_SW0	SW6	7/65
GPIO_DIP_SW1	SW6	7/65
GPIO_DIP_SW2	SW6	7/65
GPIO_DIP_SW3	SW6	7/65
GPIO_LED_0_LS	DS6	7/65
GPIO_LED_1_LS	DS5	7/65
GPIO_LED_2_LS	DS4	7/65
GPIO_LED_3_LS	DS3	7/65

Power and Status LEDs

[Figure 3, callout 30]

The following figure shows the power and status LEDs.

Figure 19: Power and Status LEDs



X27273-101422

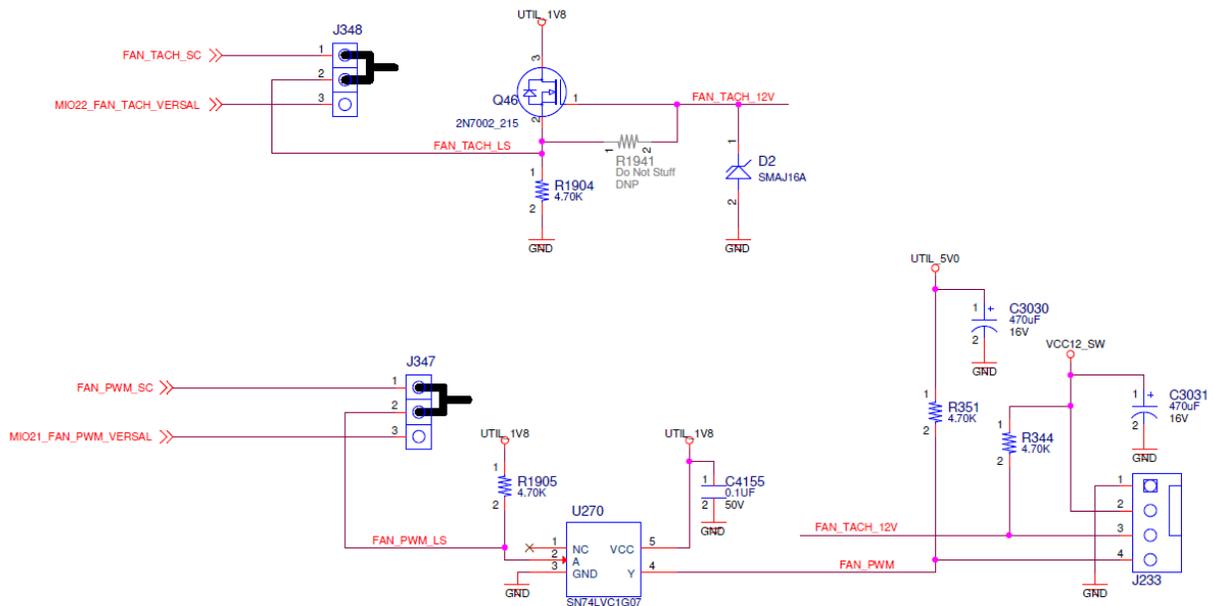
Cooling Fan Connector

[Figure 3, callout 33]

The VPK180 cooling fan connector is shown in the following figure. The VPK180 uses the system controller to autonomously control the fan speed by controlling the pulse width modulation (PWM) signal to the fan. The fan rotates slowly (acoustically quiet) when ACAP U1 is cool and rotates faster as the ACAP heats up (acoustically noisy).

The VPK180 board provides a fan controller bypass header J347 and J348 to permit control by the Versal ACAP. See the [Default Jumper and Switch Settings](#) for more details.

Figure 20: 12V Fan Header



X26028-121021

System Controller

[Figure 3, callout 49]

The VPK180 board includes an onboard system controller. The system controller hosts a website that allows for various controls over aspects of the evaluation board. This web-based interface enables the query and control of select programmable features such as clocks, FMC functionality, and power system parameters. Users should not change the default system controller image as that could potentially cause damage to the board if proper procedures are not followed. If this image needs to be updated and for more information on the system controller web interface, see the [Versal Evaluation Board System Controller Wiki](#).

The web application is shown in the following figure.

Figure 21: System Controller Web User Interface



X27293-101422

Power On/Off Slide Switch

[Figure 4, callout 18]

The VPK180 board power switch is SW13. Sliding the switch actuator from the off to the on position applies 12 VDC power from the 2x3 6-pin mini-fit power input connector J16 (power from an external 120 VAC-to-12 VDC power adapter).

★ IMPORTANT! Power to the VPK180 is mutually exclusive and only one of the two power connections should be powered. Either J16 or all of JP1, JP2, JP3, and JP4 should be used to provide board power.

The four 2x4 8-pin (6+2) ATX power supply PCIe-type connectors JP1, JP2, JP3, and JP4 are provided for higher power use cases.

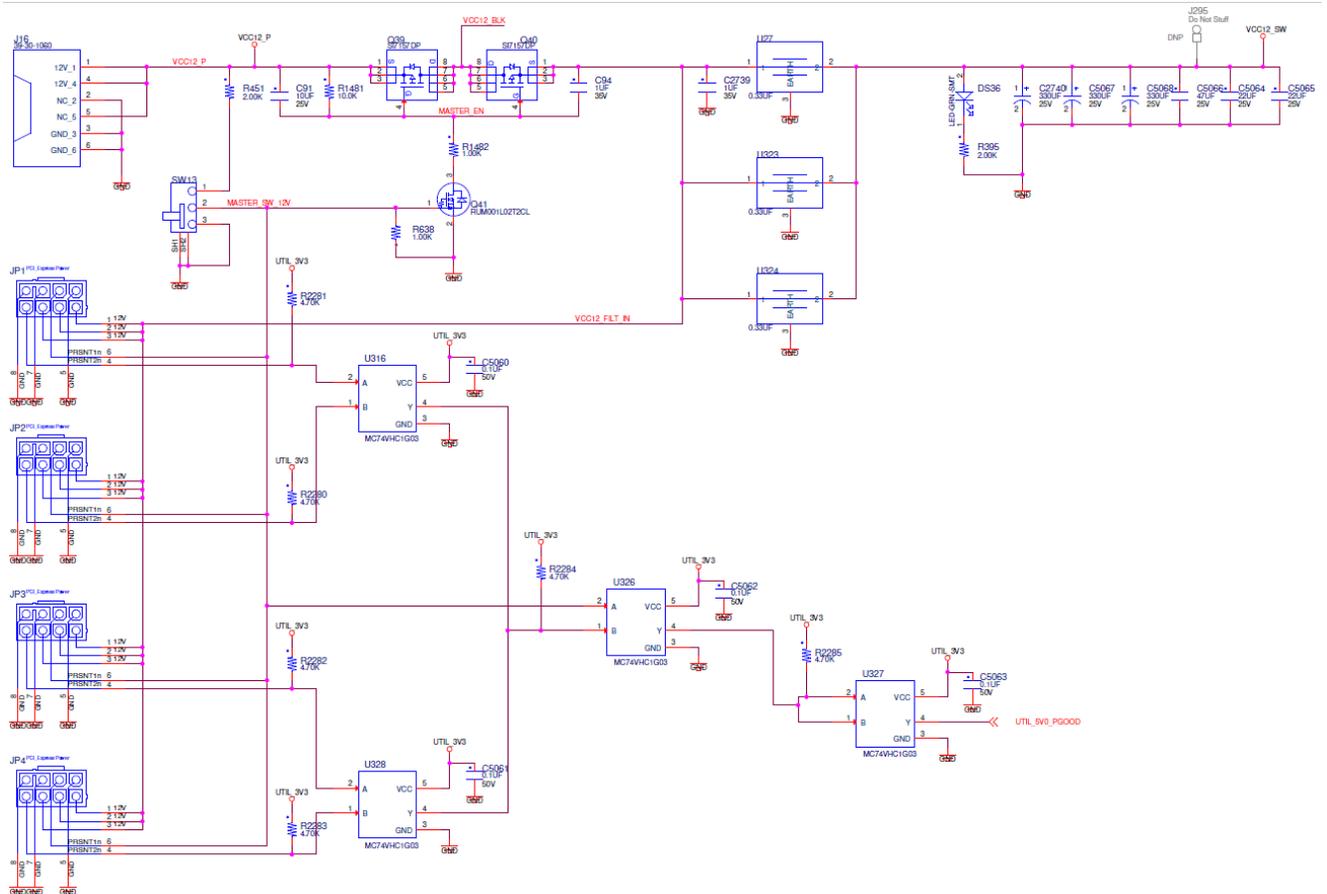
- The customer ATX supply chosen must support at least four PCIe (6+2) GPU connections to support powering the evaluation board.
- Only use a single ATX supply to support delivery of 12V to four PCIe GPU (6+2) connectors or damage might occur.
- When ATX PCIe GPU 6+2 connections are made, the 6 pin mini-fit Jr power brick connection and onboard on/off power switch is disabled.

The green LED DS36 illuminates when the VPK180 board power switch is on. See [Board Power System](#) for details on the onboard power system.

CAUTION! Do NOT plug a PC ATX power supply 6-pin connector into the VPK180 board power connector J16. The ATX 6-pin connector has a different pinout than J16. Connecting an ATX 6-pin connector into J16 damages the VPK180 board and voids the board warranty.

The following figure shows the power connector J16, power switch SW13, and LED indicator DS36.

Figure 22: Power Input



X27274-101222

Board Power System

[Figure 3, callout 18]

The VPK180 evaluation board uses power management ICs (PMIC) and power regulators from [Infineon Integrated Circuits](http://www.infineon.com) to supply the core and auxiliary voltages listed in the following tables. The detailed ACAP connections for the feature described in this section are documented in the VPK180 board schematic.

Table 20: Power System - PMBus Regulators and INA226 Map

Rail Name	Regulator Type	Ref. Des.	Vout (V)	Iout (A)	PMBUS Addr.	I2C Addr.	INA226 Ref. Des.	INA226 I2C Addr.
VCCINT	IR35215	U152	0.8	300	0x46	0x16	U65	0x40 BUS1
VCC_SOC	IR35215	U291	0.8	34	0x45	0x15	U161	0x41 BUS1
UTIL_3V3			3.3	58			N/A	N/A
VCC_PSFP	IRPS5401	U160	0.88	8	0x47	0x17	U164	0x45 BUS1
VCCO_MIO			1.8	2			U172	0x45 BUS2
VCC_PMC			0.88	2			U163	0x42 BUS1
VCC1V5			1.5	1			U264	0x43 BUS2
VCCO_502			1.8	0.5			U174	0x47 BUS2
VCC_RAM_VCCINT_GT	IRPS5401	U167	0.8	40	0x4C	0x1C	U5	0x43 BUS1
MGTVCCAUX			1.5	1			U176	0x48 BUS2
MGTAVCC			0.88	8			U265	0x42 BUS2
VCCAUX	IRPS5401	U175	1.5	18	0x4D	0x1D	U166	0x40 BUS2
UTIL_2V5			2.5	1			N/A	N/A
VCC_PSLP_CPM5			0.88	8			U165	0x44 BUS1
LPDMGTYVCCAUX			1.5	0.5			U234	0x4D BUS2
UTIL_1V8	IRPS5401	U295	1.8	1	0x48	0x18	N/A	N/A
VCCAUX_PMC			1.5	1			U168	0x41 BUS2
LPDMGTYAVCC			0.88	5			U177	0x4B BUS2
LPDMGTYAVTT	IR38060	U259	1.2	6	0x41	0x11	U260	0x4C BUS2
VADJ_FMC	IR38164	U185	1.5	6	0x4E	0x1E	U184	0x4A BUS2
VCC1V1_LP4	IR38164	U187	1.1	6	0x4F	0x1F	U186	0x49 BUS2
MGTAVTT	IR38164	U189	1.2	14	0x49	0x19	U188	0x46 BUS2

Note: Bus short names are decoded as:

- I2C Address - PMBUS_SDA/SCL
- BUS1 - PMBUS1_INA226_SDA/SCL
- BUS2 - PMBUS2_INA226_SDA/SCL

See [PMC MIO\[46:47\] I2C0 Bus](#) for I2C diagrams and more details.

The FMCP HSPC (J51) VADJ pins are wired to the programmable rail VADJ_FMC. The VADJ_FMC rail is programmed to 1.50V by default. The VADJ_FMC rail also powers the XCVC1802 FMCP interface banks 709 and 710 (see the table in [I/O Voltage Rails](#)).

Documentation describing PMBus programming for the Infineon power controllers is available on the [Infineon Integrated Circuits](#) website. The PCB layout and power system design meet the recommended criteria described in the *Versal ACAP PCB Design User Guide* (UG863).

Table 21: Power System – Non-PMBus Regulators

Rail Name	Regulator Type	Ref. Des.	Vout (V)	Iout (A)
VCC12_SW		SW13	12	Up to 50A
UTIL_5V0	IR3889	U191	5	6
SYS_VCC0V85	TPS62480	U143	0.85	5
SYS_MGTAVCC	TPS62097RWKR	U146	0.9	1
SYS_VCC1V1	TPS7A8300ARGRR	U145	1.1	1
SYS_VCC1V2	TPS62097RWKR	U147	1.2	2
SYS_VCC1V8	TPS62097RWKR	U144	1.8	1
8A34001_VCC_GPIO_DC	LP38798SD-ADJ/NOPB	U223	3.3	0.8
8A34001_VDDA	LP38798SD-ADJ/NOPB	U225	3.3	0.8
8A34001_VDDO_Q1_10_7	LP38798SD-ADJ/NOPB	U226	3.3	0.8
8A34001_VDD_CLK0	LP38798SD-ADJ/NOPB	U227	3.3	0.8
8A34001_VDDO_Q0_9_6	LP38798SD-ADJ/NOPB	U228	3.3	0.8
8A34001_VDD_CLK1	LP38798SD-ADJ/NOPB	U229	3.3	0.8
8A34001_VDDO_Q4_11	LP38798SD-ADJ/NOPB	U230	3.3	0.8
8A34001_VDDO_Q8_3_5	LP38798SD-ADJ/NOPB	U236	3.3	0.8
8A34001_OCXO_TCXO_VDD	LP38798SD-ADJ/NOPB	U243	3.3	0.8
8A34001_VDD_FOD	LP38798SD-ADJ/NOPB	U231	1.8	0.8
8A34001_VDDD	LP38798SD-ADJ/NOPB	U232	1.8	0.8
8A34001_VDDO_Q2	LP38798SD-ADJ/NOPB	U232	1.5	0.8

Note: VCC12_SW is disabled when using ATX 12V (6+2) input. Refer to the description in the [Power On/Off Slide Switch](#) introduction.

More information about the power system regulator components can be found at the [Infineon Integrated Circuits](#) website.

Monitoring Voltage and Current

Nineteen rails have a TI INA226 PMBus power monitor circuit with connections to the rail series current sense resistor. This arrangement permits the INA226 to report the sensed parameters separately on the PMBus. The rails equipped with the INA226 power monitors are shown in the power system table in [Board Power System](#). As described in [PMC MIO\[46:47\] I2C0 Bus](#), the I2C0 bus provides access to the PMBus power controllers and the INA226 power monitors via the U33 TCA9548A bus switch. All PMBus controlled Infineon regulators are tied to the PMBUS_SDA/SCL PMBus, while the INA226 power monitors are split across PMBUS1_INA226_SDA/SCL and PMBUS2_INA226_SDA/SCL.

The I2C0 bus topology figure and I2C0 port expander TCA6416A U233 address $0x20$ connections table in [PMC MIO\[46:47\] I2C0 Bus](#) document the I2C0 bus access path to the Infineon PMBus controllers and INA226 power monitor op amps. Refer to schematic for connectivity details. This can be accessed through the [VPK180 Evaluation Board](#) website. These power system components are also accessible to the ZU4 U125 system controller (bank 501) and the ACAP U1 (bank 501).

VITA 57.4 FMCP Connector Pinouts

Overview

The following figure shows the pinout of the FPGA plus mezzanine card (FMCP) high pin count (HSPC) connector defined by the VITA 57.4 FMC specification. For a description of how the VPK180 evaluation board implements the FMCP specification, see [GTYP200/201: FPGA Mezzanine Card Interface](#).

Figure 23: FMCP HSPC Connector Pinout

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PFSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	CLK3_BIDIR_P	CLK1_M2C_P	GND	HA01_P_CC	GND	DP3_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP3_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	SBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	SBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP9_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	GND	HA03_N	GND	LA00_N_CC	GND	HA05_N	GND	DP9_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_P	HA02_N	LA02_P	LA02_N	GND	HA04_P	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P
9	GND	GBTCLK3_M2C_N	HA02_N	HA02_P	LA02_N	LA02_P	GND	HA04_N	GND	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N
10	DP21_M2C_P	GND	HA05_P	HA07_N	LA04_P	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP6_M2C_P	GND	DP20_C2M_P	GND
11	DP21_M2C_N	GND	HA05_N	HA07_P	LA04_N	LA03_N	GND	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	GND	HA11_N	GND	LA08_N	GND	HA13_N	LA05_P	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_P	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	HA10_P	GND	LA07_N	GND	HA12_P	GND	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	DP6_M2C_P	GND	DP13_M2C_P	GND	GND
17	GND	SYNC_C2M_N	HA17_N_CC	HA14_P	LA11_N	LA12_P	HA15_N	HA16_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	GND	HA18_N	GND	LA16_N	GND	HA20_N	LA13_P	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	HA21_P	GND	LA15_P	GND	HA19_P	GND	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	HA22_P	LA19_N	LA20_P	HB02_N	HB03_P	GND	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	GND	HB01_N	GND	LA22_N	GND	HB05_N	LA23_P	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	HB00_P_CC	GND	LA21_P	GND	HB04_P	GND	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	HB07_P	LA24_N	LA25_P	HB08_N	HB09_P	GND	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	GND	HB11_N	GND	LA29_N	GND	HB13_N	TD0	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	HB10_P	GND	LA28_P	GND	HB12_P	GND	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	HB15_P	LA30_N	LA31_P	HB16_N	HB19_P	TRST_P	GA1	12P0V	GND	DP4_C2M_N	GND
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP16_M2C_P	GND
37	GND	12P0V	GND	HB18_N	GND	LA33_N	GND	HB21_N	3P3V	GND	DP6_C2M_N	GND	DP16_M2C_N	GND
38	DP19_C2M_P	GND	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP5_C2M_P	GND	DP5_C2M_P	GND
39	DP19_C2M_N	GND	HB17_N_CC	HB18_P	LA32_N	LA33_P	HB20_N	HB21_P	GND	12P0V	DP5_C2M_N	GND	DP5_C2M_N	GND
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_P	GND
			VIO_B_M2C	GND	VADJ	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND
													3P3V	GND

X26032-112221

Xilinx Design Constraints

Overview

The Xilinx® design constraints (XDC) file template for the VPK180 board provides for designs targeting the VPK180 evaluation board. Net names in the constraints listed correlate with net names on the latest VPK180 evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL.

See the *Vivado Design Suite User Guide: Using Constraints* ([UG903](#)) for more information.

The HSPC FMCP connectors J51 is connected to ACAP U1 banks powered by the variable voltage VADJ_FMC. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer. See [LPD MIO\[23\]: VADJ_FMC Power Rail](#) for more details on the VADJ_FMC power rail.



IMPORTANT! See the [VPK180 board documentation](#) ("Board Files" check box) for the XDC file.

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

For Technical Support, open a [Support Service Request](#).

CE Information

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

CE Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

CE Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Compliance Markings



In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

Documentation Navigator and Design Hubs

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- From the Vivado® IDE, select **Help** → **Documentation and Tutorials**.
- On Windows, select **Start** → **All Programs** → **Xilinx Design Tools** → **DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the [Design Hubs](#) page.

Note: For more information on DocNav, see the [Documentation Navigator](#) page on the Xilinx website.

References

The most up to date information related to the VPK180 board and its documentation is available on these websites:

[VPK180 Evaluation Kit](#)

VPK180 Evaluation Kit — [Master Answer Record 000033990](#)

These documents provide supplemental material useful with this guide:

1. *Versal Architecture and Product Data Sheet: Overview* ([DS950](#))
2. *Versal Premium Series Data Sheet: DC and AC Switching Characteristics* ([DS959](#))
3. *Versal ACAP Technical Reference Manual* ([AM011](#))
4. *Versal ACAP SelectIO Resources Architecture Manual* ([AM010](#))
5. *Versal ACAP PCB Design User Guide* ([UG863](#))
6. *Versal ACAP Memory Resources Architecture Manual* ([AM007](#))
7. *Versal ACAP GTY and GTYP Transceivers Architecture Manual* ([AM002](#))
8. *VPK180 System Controller Tutorial* (XTP729)
9. *Tera Term Terminal Emulator Installation Guide* ([UG1036](#))
10. *Vivado Design Suite User Guide: Using Constraints* ([UG903](#))
11. *Vivado Design Suite User Guide: Programming and Debugging* ([UG908](#))
12. *Versal ACAP System Monitor Architecture Manual* ([AM006](#))
13. *Versal ACAP Clocking Resources Architecture Manual* ([AM003](#))
14. *Versal ACAP GTM Transceivers Architecture Manual* ([AM017](#))
15. *Silicon Labs CP210x USB-to-UART Installation Guide* ([UG1033](#))
16. [Micron Technology](#) (MTA9ADF1G72AZ-3GE1, MT53D512M32D2DS)
17. [Standard Microsystems Corporation](#) (SMSC) (USB3320)
18. [SanDisk Corporation](#)
19. [SD Association](#)
20. [Skyworks/Silicon Labs](#) (SI570, SI5332, SI53340)
21. [Texas Instruments](#) (TCA9548A, TCA6416A, DP83867, PCA9306)
22. [PCI-SIG](#)
23. [Samtec, Inc.](#) (SEAF series connectors, LPAF connectors)
24. [VITA FMC Marketing Alliance](#) (FPGA Mezzanine Card (FMC) VITA 57.1, 57.4 specifications)

- 25. [Maxim Integrated Circuits \(MAX6643\)](#)
- 26. [Infineon Integrated Circuits \(IR35215, IRPS5401, IR38164, IR3897\)](#)
- 27. [Future Technology Devices International Ltd. \(FT4232HL\)](#)
- 28. [Integrated Device Technology, Inc. \(IDT\) \(8A34001, RC21008A\)](#)
- 29. [NXP Semiconductors \(NVT4857UK\)](#)
- 30. [Versal Evaluation Board - System Controller BEAM Wiki](#)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
02/21/2023 Version 1.0	
Initial release.	N/A

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