Versal ACAP System Monitor

Architecture Manual

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Chapter 1

Overview

Introduction to Versal ACAP

Versal® adaptive compute acceleration platforms (ACAPs) combine Scalar Engines, Adaptable Engines, and Intelligent Engines with leading-edge memory and interfacing technologies to deliver powerful heterogeneous acceleration for any application. Most importantly, Versal ACAP hardware and software are targeted for programming and optimization by data scientists and software and hardware developers. Versal ACAPs are enabled by a host of tools, software, libraries, IP, middleware, and frameworks to enable all industry-standard design flows.

Built on the TSMC 7 nm FinFET process technology, the Versal portfolio is the first platform to combine software programmability and domain-specific hardware acceleration with the adaptability necessary to meet today's rapid pace of innovation. The portfolio includes six series of devices uniquely architected to deliver scalability and AI inference capabilities for a host of applications across different markets—from cloud—to networking—to wireless communications—to edge computing and endpoints.

The Versal architecture combines different engine types with a wealth of connectivity and communication capability and a network on chip (NoC) to enable seamless memory-mapped access to the full height and width of the device. Intelligent Engines are SIMD VLIW AI Engines for adaptive inference and advanced signal processing compute, and DSP Engines for fixed point, floating point, and complex MAC operations. Adaptable Engines are a combination of programmable logic blocks and memory, architected for high-compute density. Scalar Engines, including Arm® Cortex®-A72 and Cortex-R5F processors, allow for intensive compute tasks.

The Versal AI Edge series focuses on AI performance per watt for real-time systems in automated drive, predictive factory and healthcare systems, multi-mission payloads in aerospace & defense, and a breadth of other applications. More than just AI, the Versal AI Edge series accelerates the whole application from sensor to AI to real-time control, all with the highest levels of safety and security to meet critical standards such as ISO26262 and IEC 61508.

The Versal AI Core series delivers breakthrough AI inference acceleration with AI Engines that deliver over 100x greater compute performance than current server-class of CPUs. This series is designed for a breadth of applications, including cloud for dynamic workloads and network for massive bandwidth, all while delivering advanced safety and security features. AI and data scientists, as well as software and hardware developers, can all take advantage of the high-compute density to accelerate the performance of any application.

The Versal Prime series is the foundation and the mid-range of the Versal platform, serving the broadest range of uses across multiple markets. These applications include 100G to 200G networking equipment, network and storage acceleration in the Data Center, communications test equipment, broadcast, and aerospace & defense. The series integrates mainstream 58G transceivers and optimized I/O and DDR connectivity, achieving low-latency acceleration and performance across diverse workloads.

The Versal Premium series provides breakthrough heterogeneous integration, very high-performance compute, connectivity, and security in an adaptable platform with a minimized power and area footprint. The series is designed to exceed the demands of high-bandwidth, compute-intensive applications in wired communications, data center, test & measurement, and other applications. Versal Premium series ACAPs include 112G PAM4 transceivers and integrated blocks for 600G Ethernet, 600G Interlaken, PCI Express® Gen5, and high-speed cryptography.

The Versal HBM series enables the convergence of fast memory, adaptable compute, and secure connectivity in a single platform. The series is architected to keep up with the higher memory needs of the most compute intensive, memory bound applications, providing adaptable acceleration for data center, wired networking, test & measurement, and aerospace & defense applications. Versal HBM ACAPs integrate the most advanced HBM2e DRAM, providing high memory bandwidth and capacity within a single device.

The Versal architecture documentation suite is available at: https://www.xilinx.com/versal.

Navigating Content by Design Process

Xilinx® documentation is organized around a set of standard design processes to help you find relevant content for your current development task. All Versal® ACAP design process Design Hubs and the Design Flow Assistant materials can be found on the Xilinx.com website. This document covers the following design processes:

- **System and Solution Planning:** Identifying the components, performance, I/O, and data transfer requirements at a system level. Includes application mapping for the solution to PS, PL, and AI Engine. Topics in this document that apply to this design process include:
  - Chapter 3: Analog Channels
  - Chapter 7: I2C or PMBus Interface

- **Hardware, IP, and Platform Development:** Creating the PL IP blocks for the hardware platform, creating PL kernels, functional simulation, and evaluating the Vivado® timing, resource use, and power closure. Also involves developing the hardware platform for system integration. Topics in this document that apply to this design process include:
  - Chapter 3: Analog Channels
  - Chapter 5: Setting Up the System Monitor
  - Chapter 7: I2C or PMBus Interface
- **System Integration and Validation:** Integrating and validating the system functional performance, including timing, resource use, and power closure. Topics in this document that apply to this design process include:
  - Chapter 3: Analog Channels
- **Board System Design:** Designing a PCB through schematics and board layout. Also involves power, thermal, and signal integrity considerations. Topics in this document that apply to this design process include:
  - SYSMON Architecture
  - Chapter 2: ADC Overview
  - Chapter 3: Analog Channels
  - Chapter 7: I2C or PMBus Interface

SYSMON Features

The System Monitor (SYSMON) provides analog-to-digital converter (ADC) functionality for monitoring internal supplies, temperature, and up to 17 channels that extend outside the device for monitoring the larger system. The SYSMON provides many features to aid in managing conversion results, such as averaging, maximum/minimum interrupts, and alarms based on configurable thresholds. Features include:

- 10-bit 200 kSPS ADC designed with a consistent sample rate of 8 kSPS regardless of the number of channels being sampled.
- Scaled ADC architecture allows up to 160 channels that can be sampled at 8 kSPS.
- Internal and external interfaces with the SYSMON:
  - Register access using the platform management controller (PMC)
  - JTAG access using the PMC
  - External I2C/PMBus interface
- Interrupt-based alarms with configurable upper and lower thresholds

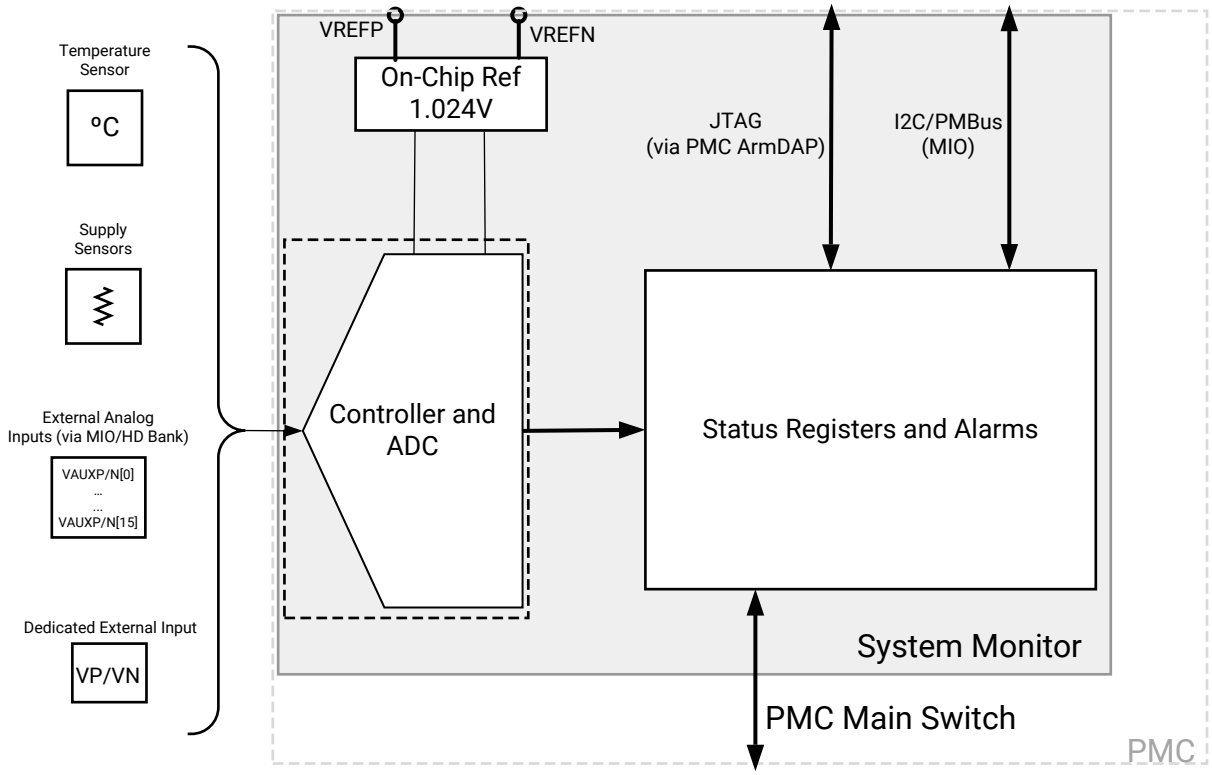
- Temperature alarm features both window and hysteresis alarm mode
- Over-temperature shutdown with configurable upper and lower thresholds
- Dedicated registers to hold maximum and minimum results for each channel being monitored
- Averaging available on all channels and sensors
- Self-calibrating ADC
- Both unipolar and bipolar monitoring of external inputs

SYSMON Architecture

The System Monitor (SYSMON) block resides in the platform management controller (PMC) where its primary function is to provide feedback on the operating conditions of the device (specifically, internal power supplies and temperature). In addition to accessing internal sensors, the SYSMON can leverage multiplexed I/O (MIO) or high-density I/O (HDIO) pins to access external pins that can monitor external channels in the wider system. The SYSMON is configured through the Vivado® Integrated Design Environment (IDE). Results are stored in a register map which connects to the PMC main switch via the advanced peripheral bus (APB) switch. The PMC main switch is an protected AXI switch that allows processor systems to access the SYSMON register map via the LPD AXI switch.

***Note*:** When a device has multiple super logic regions (SLRs), only voltages measurements in the master SLR are stored in the register map.

Figure 1: **SYSMON Block Diagram**



SYSMON Supply and Reference Requirements

There are two recommended configurations for basic pinout requirements (see SYSMON Pinout Requirements in Analog Power Supply and Ground). The SYSMON is powered from V_{CCAUX_PMC} (1.5V) and can either use an external 1.024V reference source or the internally generated on-chip reference.

It is recommended to reduce manufacturing costs by using on-chip reference for the ADC by connecting the V_{REFP} pin to GND because the external and internal references deliver similar performance in terms of accuracy and thermal drift, consult the Versal ACAP Data Sheets to see accuracy specifications when using external and on-chip reference sources. The following table lists the pins associated with the SYSMON and the recommended connectivity.

SYSMON Dedicated Pinout Requirements

The following table describes the pin functions used in the SYSMON. These are the dedicated SYSMON pins that appear in the PMC portion of the device package.

Table 1: **SYSMON Package Pins**

Package Pin	Type	Description
V_{CCAUX_SMON}	Power supply	This is the analog supply pin for the ADC and other analog circuits in the SYSMON. The pin must be tied to the 1.5V V_{CCAUX_PMC} supply. See Analog Power Supply and Ground for more information and filter considerations. This pin must never be tied to GND.
V_P	Dedicated analog input	This is the positive input terminal of the dedicated differential analog input channel (V_P/V_N). The analog input channel is very flexible and supports multiple analog input signal types. For more information, see External Analog Inputs. This pin must be connected to GND_SMON if not used.
V_N	Dedicated analog input	This is the negative input terminal of the dedicated differential analog input channel (V_P/V_N). The analog input channel is very flexible and supports multiple analog input signal types. For more information, see External Analog Inputs. This pin must be connected to GND_SMON if not used.
GND_SMON	Power supply	This is the ground reference pin for the ADC and other analog circuits in the SYSMON. It can be tied to the system ground with an isolating ferrite bead as shown in the SYSMON Pinout Requirements figure in Analog Power Supply and Ground. In a mixed-signal system, this pin must be tied to an analog ground plane (if available), in which case the ferrite bead is not required. See Analog Power Supply and Ground for more information.
V_{REFP}	Reference voltage input	This pin can be tied to an external 1.024V accurate reference IC. It must be treated as an analog signal that together with the V_{REFN} signal provides a differential 1.024V voltage. By connecting this pin to GND_SMON, an on-chip reference source is activated (see the SYSMON Pinout Requirements figure in Analog Power Supply and Ground. This pin must be connected to GND_SMON if an external reference is not supplied. See Reference Inputs (V_{REFP} and V_{REFN}) for more information.
V_{REFN}	Reference voltage input	This pin must be tied to ground pin of an external 1.024V accurate reference IC. It must be treated as an analog signal that, together with the V_{REFP} signal, provides a differential 1.024V voltage. This pin must always be connected to GND_SMON even if an external reference is not supplied. See Reference Inputs (V_{REFP} and V_{REFN}) for more information.
I2C_SCLK/SMBCLK	SYSMON I2C/PMBUS ports that can be assigned to multi-function MIO pins	Optional I2C/PMBUS port that can be used to support the I2C or PMBUS interface to the SYSMON. Only active when I2C/PMBUS interface is used.
I2C_SDA/SMBDAT	SYSMON I2C/PMBUS ports that can be assigned to multi-function MIO pins	Optional I2C/PMBUS port that can be used to support the I2C or PMBUS interface to the SYSMON. Only active when I2C/PMBUS interface is used.

Table 1: **SYSMON Package Pins** *(cont'd)*

Package Pin	Type	Description
SMBALERT	SYSMON PMBUS ports that can be assigned to multi-function MIO pins	Optional PMBus alert. When low, indicates a system fault that must be cleared using PMBUS commands. Only active when PMBUS interface is used.

Differences from Previous Generations

The SYSMON block has been redesigned in Versal® architecture to give full-featured support for all supply sensors. In Versal architecture, the SYSMON only exists in the processing system (PS) block as a feature of the platform management controller (PMC), with measurement capability extending across the whole device. Internal access to the SYSMON readings register map are available through memory-mapped registers, which can also be accessed through the external JTAG, I2C, or PMBus interfaces. Additional differences include:

- Samples are stored in PMC memory-mapped registers. There is no dedicated interface to the SYSMON through the PL.
- Scaled ADC architecture allows 160 channels sampling capability at 8 kSPS.
- The ADC architecture is scaled such that regardless of how many channels are monitored, an 8 kSPS sample rate can be achieved.
- Register-based status bits with interrupt capability inform the availability of new results, replacing PL based EOS and EOC status ports in previous architectures.
- External analog inputs are available in multiplexed I/O (MIO) and high-density I/O (HDIO) banks.
- External analog input selection is completely flexible within a MIO or HDIO bank, meaning that there are not strict channel pairs (i.e., any pin in the same MIO or HDIO bank can be a P or N side associated with any other pin in the same bank).
- All internal supply and bank voltages can be monitored.
- All channels are full-featured with unique alarm thresholds and averaging.
- Alarms are interrupt-capable status registers rather than dedicated signal ports
- The configuration of the SYSMON must be controlled by the Control, Interface, and Processing IP in Vivado tools.
- There are no fixed results register locations per channel. Registers are assigned to channels by the Control, Interface, and Processing IP in Vivado.
- The temperature transfer function is internally applied and results are stored in signed, fixed-point format, Q8.7, directly reading Celsius.
- Supply samples stored in floating-point format, directly reading voltage.

- Shared-N and bus ground features reduce the package pins requirement for auxiliary analog inputs by sharing reference pins for unipolar operation.
- PMBus and I2C interfaces are available only after the SYSMON has been configured.
- PMC provides access to results through JTAG and AXI interfaces.
- Dynamic reconfiguration port (DRP) access and dedicated alarm ports are no longer supported.
- Improved noise immunity provides more accurate sampling when using internal reference.
- Provides averaging function of up to 16 samples on all channels.

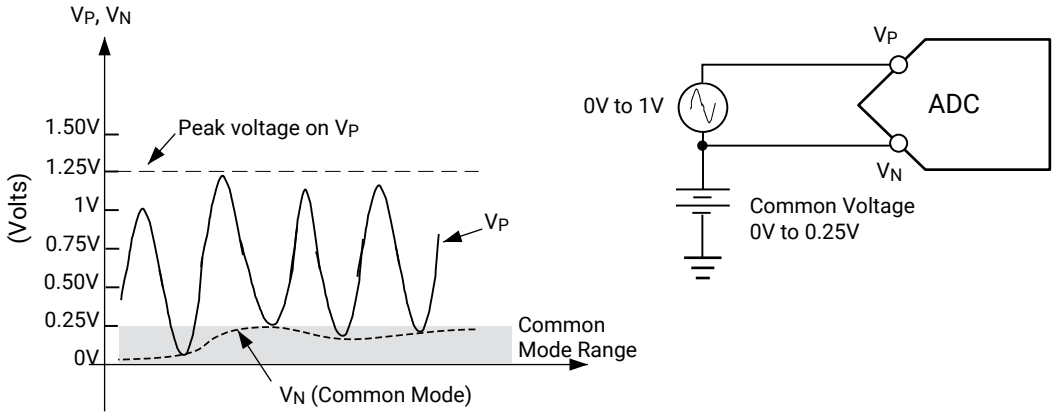
ADC Overview

The System Monitor (SYSMON) block contains a 10-bit, 0.2 MSPS analog-to-digital converter (ADC). The SYSMON has access to internal sensors to measure temperature and user supplies across the device. Additionally, the SYSMON has access to external pins to measure voltage levels external to the device. The SYSMON has a dedicated V_P/V_N pin pair and can connect to up to 16 external analog pins in MIO or HDIO pins. The SYSMON leverages a self-calibrating ADC to accommodate both unipolar and bipolar modes to sample external inputs. The SYSMON results are accessible through a register map interface in the platform management controller (PMC). All samples are stored in a floating-point format.

Unipolar Mode

When measuring positive external channels or when the SYSMON measures internal sensors, the ADC operates in a unipolar mode. In this mode, the ADC negative input terminal (V_N) must always be lower than the ADC positive input terminal (V_P). In this mode, the voltage on V_P measured with respect to V_N must always be positive. The V_N input should always be driven by an external analog signal. V_N is typically connected to a local ground or common mode signal. The common mode signal on V_N can vary from 0V to +0.25V (measured with respect to GND). Because the differential input range is from 0V to 1.0V (V_P/V_N), the maximum signal on V_P is 1.25V. See the following figure.

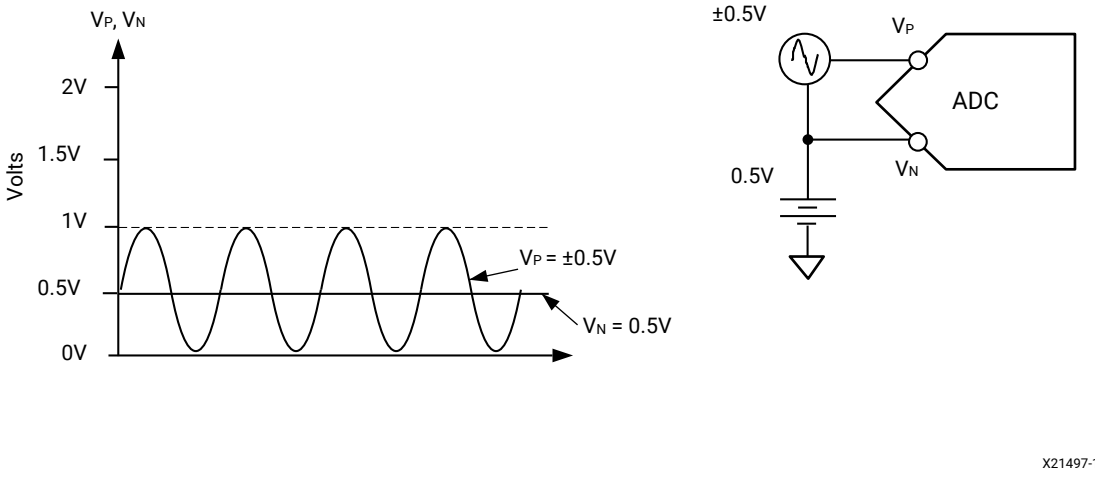
Figure 2: **Unipolar Input Signal Range**



Bipolar Mode

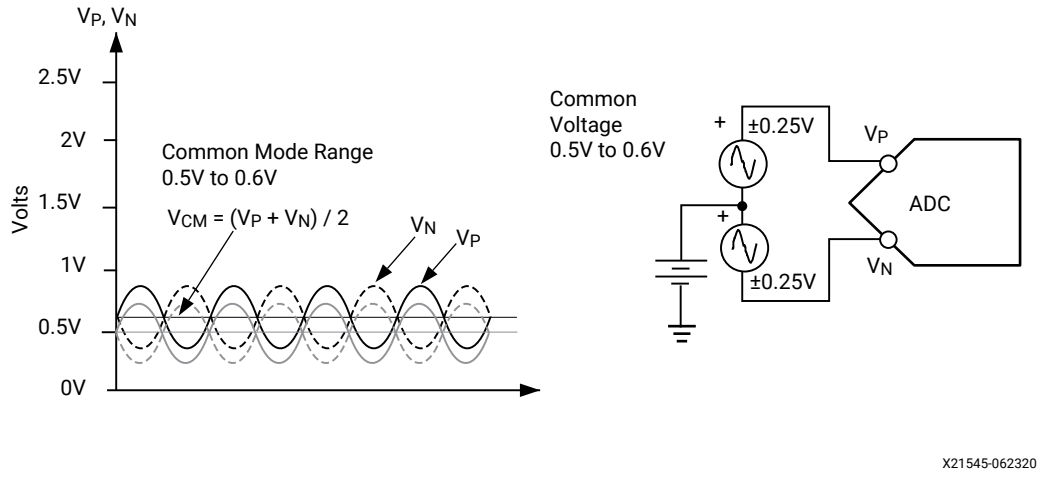
The analog inputs can accommodate analog input signals that are positive and negative with respect to a common mode or reference. To accommodate these types of signals, the analog input must be configured to bipolar mode. All input voltages must be positive with respect to analog ground (GND). When bipolar operation is enabled, the differential analog input (V_P–V_N) can have a maximum input range of ±0.5V. The common mode or reference voltage should be between 0.5V and 0.6V in this case. The SYSMON data format accommodates both positive and negative signaling, so a sign bit is always incorpoated into the results register, allowing a common format between unipolar and bipolar samples. See the following figure.

Figure 3: **Bipolar Input Signal Range**



The bipolar input mode also accommodates input signals driven from a true differential source, for example, a balanced bridge. In this case, V_P and V_N can swing positive and negative relative to a common mode or reference voltage (see the following figure). The maximum differential input (V_P–V_N) is ±0.5V. With maximum differential input voltages of ±0.5V and assuming balanced inputs on V_N and V_P, the common mode voltage must lie in the range 0.5V to 0.6V as shown in the figure below.

Figure 4: **Differential Input Signal Range**



ADC Data

To accommodate diverse needs of a system, the ADC has many operating modes. The ADC can accommodate channels of different voltage scales, external measurement modes, and data types (i.e., temperature and voltage). To simplify the user interface, the ADC has been designed to internally accommodate different use cases and store the captured data in the common floating-point format scaled to the appropriate value.

In Versal® architecture, the SYSMON result register stores all external and internal voltage measurements in a floating-point format that contains sign and format bits, a pair of exponent offset bits, and 16 bits of ADC data. This eliminates the need to apply transfer functions or to understand the scale of the ADC data and allows a common format to be used for all voltage measurements.

The SYSMON stores internal temperature sample results in a fixed-point format already transferred from the sensor's voltage format to degrees Celsius. The fixed-point format leverages a fixed seven fractional bits format to provide a signed result in degrees Celsius.

See Chapter 3: Analog Channels for details on the various data format types stored in the memory-mapped registers.

Internal Calibration

The SYSMON ADC is self-calibrating and automatically ensures regular calibration sequences are enabled whenever the SYSMON is enabled. Internal calibration ensures the accuracy of the ADC results when using either external reference or internal reference.

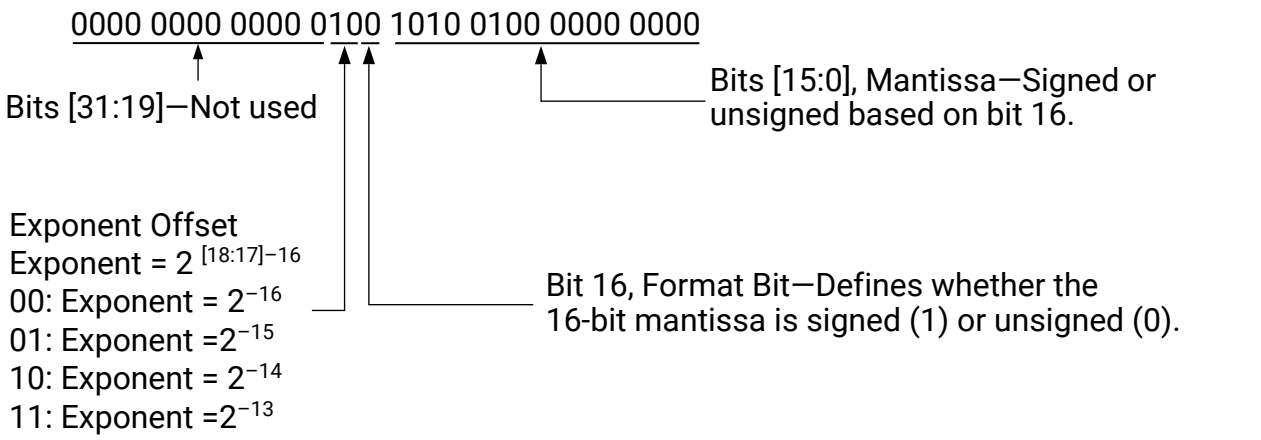
Analog Channels

To monitor the system's operating environment, the System Monitor (SYSMON) is equipped with supply sensors, temperature sensor, and external inputs that connect the ADC off-chip. All ADC readings are stored in the SYSMON memory-mapped registers that is defined by the Control, Interface, and Processing (CIPS) IP in Vivado® tools. Because the quantity and type of sensors available in a device vary by device, the CIPS IP is device-aware and equipped to enable specific sensors. The CIPS IP automatically maps the selected voltage sensor to the SYSMON registers by assigning a SUPPLY number (referred to generically as XX in this manual) to a given channel number. The supply number is maintained across all references to a supply. In Xilinx Versal® ACAPs, with monitoring the maximum number of channels (160), readings can still be provided at a rate of at least 8 kSPS. For a list of SYSMON registers and their function, see *Versal ACAP Register Reference* (AM012).

Analog Voltage format

All registers holding voltages, including measurements and thresholds, are represented in a 19-bit modified floating-point format, directly reading in units of Volts. The sample data is stored in the least significant 19 bits of a 32-bit sample register. The sixteen least significant bits represent the mantissa of the sample in either a signed or unsigned format. The format bit (bit 16) defines whether the mantissa is signed (1) or unsigned (0). Bits 17 and 18 define the scaling of the mantissa. See the following figure.

Figure 5: **General Voltage Format**



Supply Sensors

The SYSMON includes on-chip sensors that allow monitoring of the device power-supply voltages using the ADC. All externally supplied power rails have an associated sensor, which can analyze any supply that might be critical to a system. Supply sensors sample and attenuate the power supply voltages to be compatible with the ADC operating requirements. The results of internal supply sensors are appropriately scaled and stored in the channel's data register in a floating-point voltage format. There are two types of supply sensors—Supply and Supply Extended. The Supply Extended range is used to sample supply voltages greater than 1.8V, i.e., HDIO bank supply voltage. Selecting the appropriate mode is automatically determined by the processor configuration IP. The Supply Sensor data format is defined in the Supply Sensor Data Format section.

IMPORTANT! *The SYSMON measures supply rails at the die level, while the data sheet supply requirements are given at the package ball. Because the DC resistance through the package can cause a supply's level to drop after it reaches the SYSMON sensor, IR drop must be accounted for when setting alarm thresholds.*

In general, all externally generated supplies are available to be monitored by the SYSMON with no limitations other than the 160 channel register locations for storing results. All sensors are equipped with the same channel features defined in Chapter 4: Channel Features.

The following table provides some common supplies that can be enabled by the Control, Interface, and Processing IP by block type.

Table 2: **Commonly Available Sensors by Block**

Block Type	Supply Sensors Available
PL core supplies	V_{CCAUX}, V_{CCINT}, V_{CC_RAM}
PS core supplies	V_{CCINT_PMC}, V_{CCAUX_PMC}, V_{CC_PSLP}, V_{CC_PSFP}, V_{CC_SOC}, V_{CC_BAT}
SelectIO™ interface bank supplies and PSIO bank Voltages	V_{CCO}, V_{CC_IO}
MGT supplies	GTY_AVCC, GTY_AVCCAUX, GT_AVTT

Supply Sensor Data Format

The least significant 19 bits of a supply sensor's 32-bit register contain sensory readings in a floating point format. All supply sensor data is stored in an unsigned format, an exponent of 2^{-15} or 2^{-14} (for extended range supplies, i.e., HDIO bank voltage sensors). Extended range supplies are stored with a 2^{-15} exponent and include all sensors with supplies that can exceed 1.6V, namely HDIO banks.

Figure 6: **Supply Mode Example**

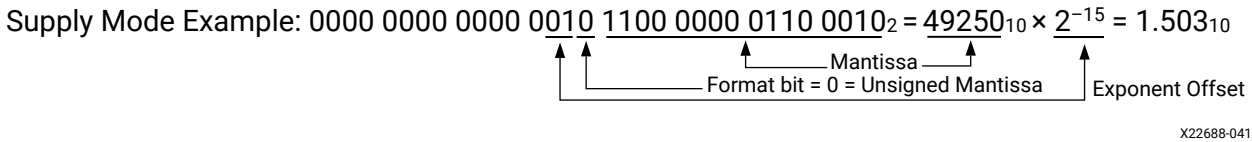
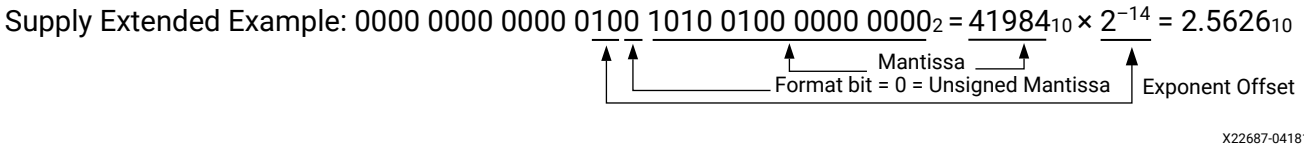


Figure 7: **Supply Extended Example**



External Analog Inputs

The System Monitor provides access to 17 external analog channels. The V_P/V_N are dedicated external analog pins, while the SYSMON can also accommodate up to 16 external analog pins on multiplexed I/O and high-density I/O (PS/PMC MIO and HDIO) pins. These 16 external analog pins are referred to as auxiliary input pins (VAUXP[15:0]/VAUXN[15:0]) and connect the ADC to external pins on the device through a set of MIO pins or the HDIO pins (not present in all devices).

For an external auxiliary channel, pin selection is extremely flexible and can leverage pins in the same bank or spread out amounts on multiple PS/PMC MIO and HDIO banks (when applicable). Any two pins within a capable bank can be paired for a given external auxiliary channel and can operate in unipolar mode or bipolar mode. An auxiliary channel can share VAUXN pins or can use the bank's ground as the VAUXN pin (for unipolar sampling only). The Control, Interface, and Processing IP in the Vivado tool is used to assign auxiliary external analog inputs and ensure that I/O pins used by the SYSMON are prohibited from being used as user I/O in the Vivado tool. For a description of the external analog input's equivalent analog circuit, see the Analog Input Description section.

Shared-N

To minimize the package pins required to sample an external channel, the auxiliary analog inputs can support single-pin sampling. Typically useful when measuring several channels with a common reference, VAUXN pins can be used as a reference for multiple VAUXP channels, known as shared-N. When using the shared-N mode, the number of package pins required to support 16 auxiliary analog inputs can be reduced from 32 package pins to 17. Any pin used in VAUXN in an auxiliary channel can be used as a VAUXN reference for any other channel in the same bank. There are no restrictions on how many channels can share a VAUXN channel or how many VAUXN channels can be shared.

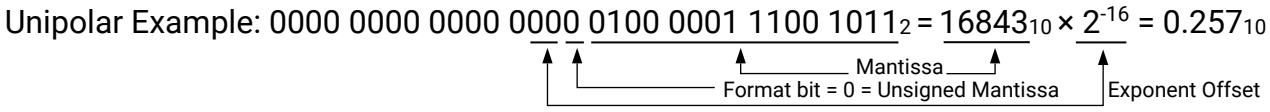
Bank Ground

When only unipolar mode is required on an auxiliary analog input, the bank ground feature allows for VAUXN to be internally connected to ground of the bank in which the VAUXP pin is located. Using bank ground can be convenient for monitoring external references that share ground, while preserving the highest amount of pins for other user I/O functions. Bank ground is enabled in the CIPS wizard when configuring an external reference with a AUX_IO_N port on a channel to the AUX_IO_P's bank ground.

External Analog Inputs Data Format

The least significant 19 bits of an external analog input's result register store sensor data in a floating-point format. The following equation describes an example of converting external analog input data formats.

Figure 8: **External Voltage Format Unipolar**



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***Note*:** In the above example, only the 16 LSBs of the 19-bit format are listed. The bits 18:16 are not part of the mantissa and thus are fixed for a given format type.

Temperature Sensor

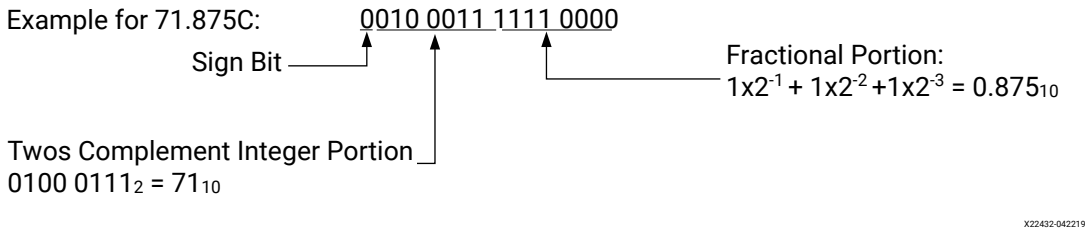
The SYSMON contains a temperature sensor that produces a voltage output proportional to the die temperature. The SYSMON internally scales the captured voltage and stores the data in the appropriate temperature data register, converted to a signed Q8.7 fixed-point Celsius format. SYSMON presents the temperature to the user primarily through the DEVICE_TEMP_MAX register. This reading must be used when considering operating junction temperature. It is recommended that Vivado versions 2021.1 and greater are used to generate SYSMON designs to avoid wider than expected temperature variation as described in Xilinx Answer Record 76641.

Temperature Data Format

The SYSMON leverages the Q fixed-point number format to provide a signed temperature value stored in the Celsius scale. Temperature information is stored in the 16 least significant bits of the register in a Q8.7 signed format. The Q8.7 format consists of a sign bit, 8 integer bits, and 7 fractional bits.

***Note*:** The SYSMON temperature results are automatically converted to Celsius. There is no scaling or transfer function. See the following figure.

Figure 9: **Temperature Data Format**



The following equations show converting the SYSMON format between decimal and the Q8.7 format SYSMON uses for both temperature readings and alarms.

Converting 71.875C Q8.7 Temperature Format to Decimal

$$0010\ 0011\ 1111\ 0000_2 = 9200_{10} = 9200_{10}\text{V} \div 2^7 = 71.875_{10}\text{C}$$

Converting 71.857V Decimal to Q8.7 Temperature Format

$$71.875_{10}\ \text{C} \times 2^7 = 9200_{10} = 0010\ 0011\ 1111\ 0000_2\ \text{C}$$

Channel Features

Every channel in the System Monitor (SYSMON) can leverage several features that enable the conversions captured by SYSMON to be more convenient to use.

- Averaging—Each channel can be uniquely enabled with an averaging rate of 2, 4, 8, and 16 conversions.
- Max/Min Tracking—Each channel stores the maximum and minimum samples captured by the SYSMON since the last reset.
- Alarms—Up to 160 channels can be configured to assert alarms and interrupts based on user-defined thresholds.

In addition, the temperature monitor channel can be configured to trigger a shutdown of the system when the device is operating in an unexpected or undesired temperature range.

Averaging

Averaging can be used to filter ADC voltage samples. All SYSMON channels can independently have averaging enabled, but must share the same averaging level of 2, 4, 8, or 16 samples. Channels that have averaging enabled only have the results register updated when an averaging sequence is complete (i.e., once every 2, 4, 8, or 16 samples). All other features that use sensor readings only act on an averaged value, not individual samples, when averaging is enabled. The CIPS wizard allows the user to set an averaging level and enable check boxes for per channel enabling of the averaging function. Averaging can also be set in the SYSMON_PMC CONFIG register which is described in the *Versal ACAP Register Reference* (AM012).

Note: Although voltage averaging can be enabled on per channel basis, the averaging level is restricted to the same for all channels that have averaging enabled.

Even though all voltage channels must share the same averaging level, the temperature sensor will not be impacted by voltage averaging settings.

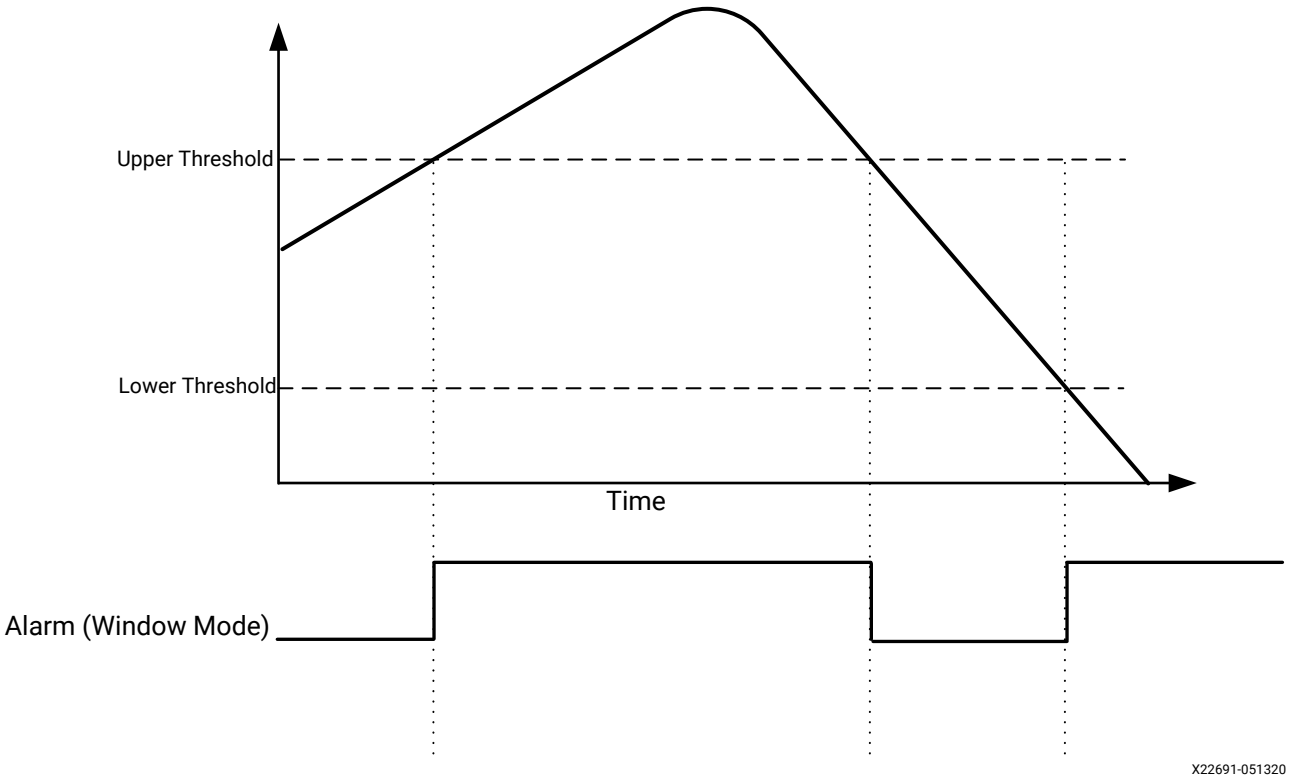
Maximum/Minimum Tracking

The SYSMON maintains a pair of registers for each enabled channel to store the maximum (SUPPLYXX_MAX) and minimum (SUPPLYXX_MIN) values sampled since the last reset. If a given channel has averaging enabled, the maximum and minimum registers only update with averaged noise-filtered readings, rather than the max/min for a single sample. With the STATUS_RESET register, individual supplies' maximum and minimum registers can be uniquely reset. These registers are described in the SYSMON _ROOT module of the *Versal ACAP Register Reference* (AM012).

Alarms

Along with two temperature alarms (device and over-temperature) all the SYSMON can assert one up to 160 available voltage alarms (supply or external channels) in the system. Alarm assertion levels are fully customizable and interrupts can be enabled for both temperature alarms and voltage alarms. When averaging is enabled for an alarm, the alarm always asserts on the averaged value, rather than a single sample.

Figure 10: **Voltage Alarm Behavior**



Voltage Alarms

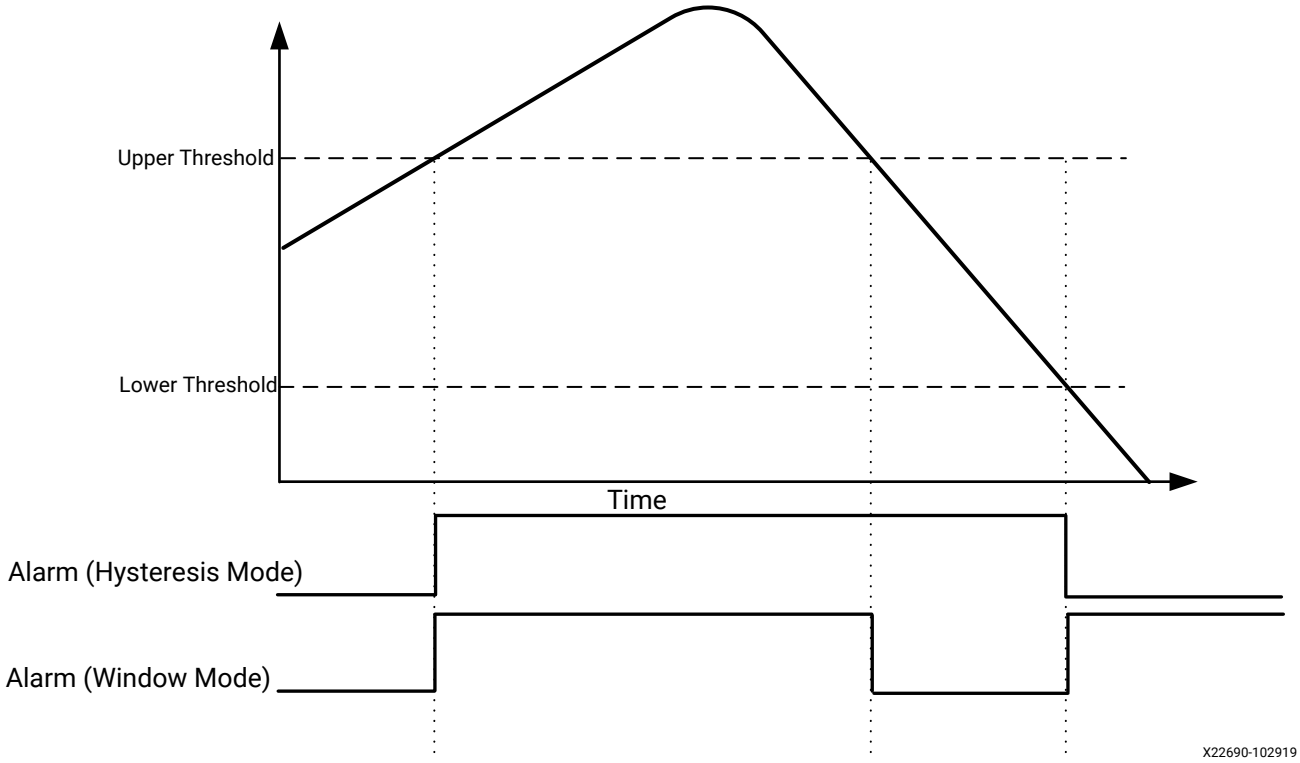
Alarms enabled for voltage monitoring (supply and external inputs) commonly use window mode, in which the alarm is asserted if a reading falls above the upper threshold or below the lower threshold (see the previous figure). The CIPS wizard offers a GUI to configure the various registers used to set thresholds and enable alarms, SUPPLY0_TH_UPPER through SUPPLY159_TH_UPPER, SUPPLY0_TH_LOWER through SUPPLY159_TH_LOWER, ALARM_CONFIG, ALARM_REG0 through ALARM_REG5. Alarm assertion is indicated through the ALARM_FLAG0 through ALARM_FLAG4 and interrupts can be enabled to indicate an alarm occurrence. For additional details on these registers, see the Chapter 6: SYSMON Registers section and refer to the SYSMON_PMC module in the *Versal ACAP Register Reference* (AM012).

Temperature Alarms

Because temperature concerns tend to be related to over-temperature, the temperature alarm typically uses the alarm mode called Hysteresis mode. Hysteresis mode asserts the alarm above a high temperature threshold, but uses the lower alarm threshold to deassert the alarm. This can be convenient in applications that reduce device function at high temperature only to resume when a sufficiently cool device temperature is achieved. See the following temperature alarm behavior diagram for an illustration of the alarm assertion behavior. As with voltage mode alarms, averaged values trigger alarm behavior.

Unlike the voltage alarms, the temperature alarms are always enabled and have a dedicated alarm register. Temperature Alarms are asserted in the REG_ISR register, while DEVICE_TEM_TH_LOWER, DEVICE_TEMP_TH_UPPER, OT_TEMP_TH_LOWER and OT_TEMP_TH_UPPER define the temperature alarm behavior. For additional details on these registers and associated drivers, see the Chapter 6: SYSMON Registers section and refer to the SYSMON_PMC module in the *Versal ACAP Register Reference* (AM012).

Figure 11: **Temperature Alarm Modes**



Over-Temperature Shutdown

When the device temperature exceeds a user-defined temperature threshold, the over-temperature (OT) alarm becomes active. When OT shutdown is enabled, the OT alarm in the PMC asserts to indicate over-temperature condition has occurred. The OT_TEMP_TH_LOWER and OT_TEMP_TH_UPPER registers dictate thresholds while the ALARM_CONFIG register controls the alarm behavior. For additional details on these registers and associated drivers, see the Chapter 6: SYSMON Registers section and refer to the SYSMON_PMC module in the *Versal ACAP Register Reference* (AM012).

IMPORTANT! *Starting in Vivado 2021.2, the error response to the OT shutdown alarm is set by the CIPS wizard. By default, the CIPS asserts SRST when the OT alarm is asserted.*

Setting Up the System Monitor

Application Guidelines

The SYSMON is a precision analog measurement system based on a 10-bit analog-to-digital converter (ADC) with an LSB size approximately equal to 1 mV. To achieve the best possible performance and accuracy with all measurements (both on-chip and external), several dedicated pins for the ADC reference and power supply are provided. When connecting these pins, follow the guidelines in this chapter to ensure the best possible performance from the ADC. This chapter outlines the basic design guidelines to consider as part of the requirements for board design.

Reference Inputs (V_{REFP} and V_{REFN})

Improved noise immunity, ensures that the performance of the on-chip reference provides a similar accuracy to an externally supplied reference. The SYSMON on-chip reference option that is selected by connecting V_{REFP} and V_{REFN} to ADCGND as shown in the following figure. The performance with on-chip and internal reference are specified in the Versal ACAP Data Sheets.

The V_{REFP} and V_{REFN} high-impedance inputs can be used to deliver a differential reference voltage for the analog-to-digital conversion process. Errors in the reference voltage affect the accuracy of absolute measurements for both on-chip sensors and external channels because the ADC is only as accurate as the reference provided. Noise on the reference voltage also adds noise to the ADC conversion and results in more code transition noise or poorer than expected SNR. For typical usage, the reference voltage between V_{REFP} and V_{REFN} should be maintained at 1.024V ± 0.2% using an external reference IC. Reference voltage ICs that deliver 1.024V are widely available from several vendors.

RECOMMENDED: *The 1.024V reference should be placed as close as possible to the reference pins and connected directly to the V_{REFP} input, using the decoupling capacitors recommended in the reference IC data sheet. The recommended reference connections are illustrated in SYSMON Supply and Reference Requirements.*

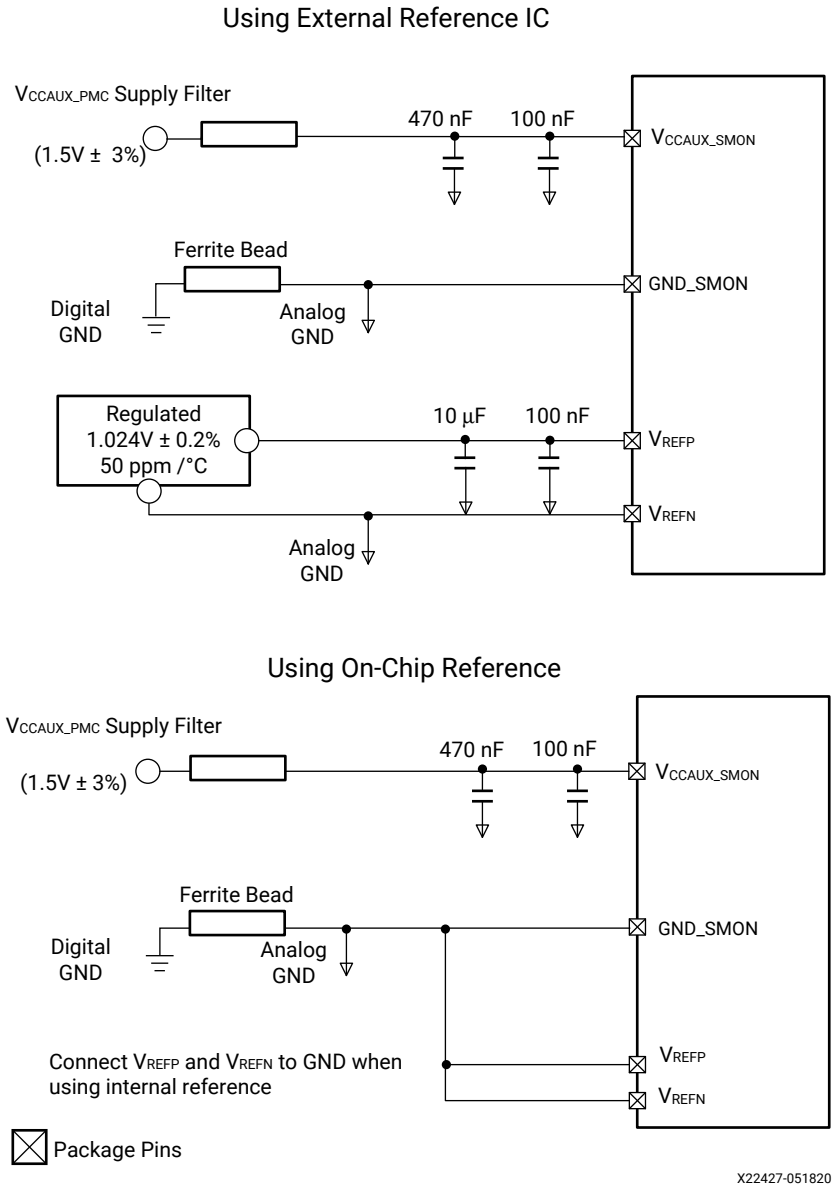
Analog Power Supply and Ground

The analog power supply (V_{CCAUX_SMON}) and ground (GND_SMON) inputs provide the power supply and ground reference for the analog circuitry in the SYSMON. A common mechanism for the coupling of noise into an analog circuit is from the power supply and ground connections. Excessive noise on the analog supply or ground reference affects the ADC measurement accuracy. For example, I/O switching activity can cause significant disturbance of the digital ground reference plane. Thus, it is not advisable to use the digital ground as an analog ground reference for SYSMON.

Similarly, for the digital supplies for the interconnect logic, high switching rates easily result in high-frequency voltage variations on the supply, even with decoupling. To mitigate these effects on ADC performance, a dedicated supply and ground reference is provided. The following figure illustrates how to use the 1.5V V_{CCAUX_PMC} supply to power the analog circuitry. V_{CCAUX_PMC} is filtered using a low-pass network. The filter design depends on the ripple and ripple frequency (if any) on the V_{CCAUX_PMC} supply if, for example, a switching regulator is used. There is also a power-supply rejection specification for the external reference circuit to consider. The filtering should ensure no more than 1 LSB (1 mV) of noise on the reference output to minimize any impact on ADC accuracy at 10 bits. Depending on the ripple frequency of the supply, a 10–20 µH inductor might be better than a ferrite bead.

In mixed-signal designs it is common practice to use a separate analog ground plane for analog circuits to isolate the analog and digital ground return paths to the supply. Common ground impedance is a mechanism for noise coupling and needs to be carefully considered when designing the PCB. Although a separate analog ground plane is recommended for 10-bit operation, it is often not possible or practical to implement a separate analog ground plane in a design. For example, if only the on-chip sensors are used, one low-cost solution is to isolate V_{REFN} and GND_SMON ground references (such as a trace) from the digital ground (plane) using a ferrite bead as shown in the following figure.

Figure 12: **SYSMON Pinout Requirements**



IMPORTANT! *It is also important to place the 100 nF decoupling capacitors as close as possible to the package balls to minimize inductance between the decoupling and package balls.*

The ferrite bead behaves like a resistor at high frequencies and functions as a lossy inductor. The ferrite helps provide high frequency isolation between digital and analog grounds. Though it is recommended to use the on-chip reference, when using the external reference, an IC maintains a 1.024V difference between V_{REFP} and V_{REFN}. The ferrite offers little resistance to the analog DC return current. The reference inputs should be routed as a tightly coupled differential pair from the reference IC to the package pins. If routed on the same signal layer, the supply and analog ground traces (V_{CCAUX_SMON} and GND_SMON) must be used to shield the reference inputs because they have a higher tolerance to any coupled noise.

Analog Input Description

In Versal architecture, the SYSMON analog input channels consist of a sampling switch and sampling capacitor used to acquire the analog input signal for a conversion. During the ADC acquisition phase, the sample switch is closed and the sampling capacitor is charged up to the voltage of the analog input. The sampled signal must settle during the acquisition phase, which is 1.6 µs, with an additional sampling period (3.4 µs) of settling time present when using an external multiplexer. The ADC has 10-bit resolution, so to allow for margin, 12-bit settling of the input signal is targeted during the acquisition phase. To ensure adequate settling time, a maximum total source impedance of 5 kΩ for dedicated and auxiliary inputs to ensure adequate settling times. When using an anti-aliasing filter, note that the impedance of the filter adds to the source impedance so care must be taken to ensure that the total remains within the limit.

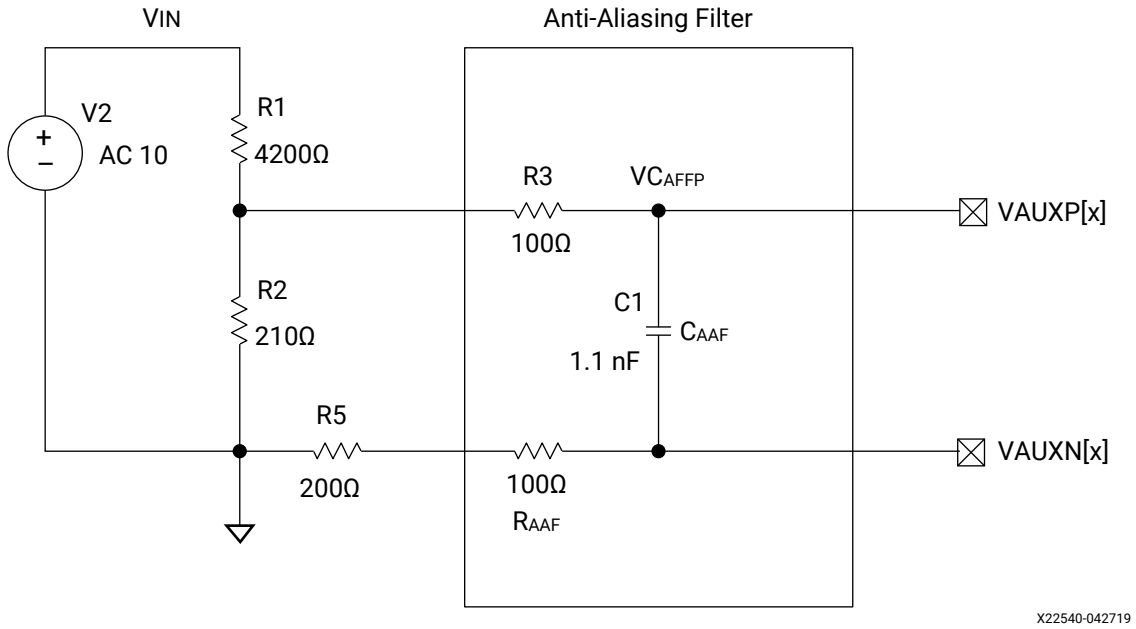
Any additional external resistance, such as the anti-alias filter or resistor divider, increases the acquisition time requirement due to the increased RMUX value in the first equation. When using an anti-aliasing filter, the additional loading it presents to the input signal reduces the max source impedance, to achieve 12-bit settling, to 700Ω.

For more information and design considerations for driving the ADC inputs, see *Driving the Xilinx Analog-to-Digital Converter* (XAPP795).

Considerations for External Analog Inputs

The analog inputs are high-impedance differential inputs. The differential input scheme enables the rejection on common mode noise on any externally applied analog-input signal. The input AC impedance is typically determined by the sensor, the output impedance of the driving circuitry, or other external components because of the high impedance of each input (such as V_P and V_N). The following figure illustrates a simple resistor divider network that is used to monitor and reduce a higher voltage supply rail to be compatible with the ADC input voltage range in unipolar input mode. To ensure that noise coupled onto the analog inputs is common to both inputs (reduce differential noise), the impedance on each input must be matched. Analog-input traces on the PCB must also be routed as tightly coupled differential pairs.

Figure 13: **Anti-Alias Filter and Voltage Attenuation**



Also shown in the figure above is a low-pass filter network at the analog differential inputs. This filter network is commonly referred to as the anti-alias filter and must be placed as close as possible to the package pins. The sensor can be placed remotely from the package as long as the differential input traces are closely coupled. The anti-alias filter attenuates high-frequency signal components entering the ADC where they could be sampled and aliased, resulting in ADC measurement corruption. As shown in the figure above, resistors R1 and R2 can divide the 10V supply down to 0.5V to work with the SYSMON. R5 has been impedance matched to the parallel resistance of R1 and R2. See *Driving the Xilinx Analog-to-Digital Converter* (XAPP795) for additional details. A discussion of aliasing in sampled systems is beyond the scope of this document.

Over and Under Voltages

The input voltage can exceed V_{CCAUX_SMON} (1.5V) or go below GND_SMON by as much as 100 mV without damage to the SYSMON. A current-limiting resistor of at least 100Ω must be placed in series with the analog inputs to limit the current to 1 mA. The resistors in the anti-alias filters fulfill this requirement. If the analog input range (1V) is exceeded, the ADC output code clips at the maximum output code.

Configuring the SYSMON

To provide a comprehensive system monitoring solution in the Versal ACAP architecture, configuring the SYSMON needs device specific knowledge and a non-dedicated channel configuration. With this in mind, it is required that the control, interface, and processing system (CIPS) IP in Vivado tools are used to enable and configure the SYSMON. The CIPS IP provides a GUI interface to set alarms, enable averaging, and enable I2C/PMBus access.

The CIPS IP wizard provides many functions to configure Versal ACAP designs, but access for the SYMON configuration if found under the "device integrity options" section of the user interface. The SYSMON configuration portion of the CIPS wizard is broken down into the following tabs.

- Basic Configuration
- On-Chip Supply Monitor
- Temperature
- External Supply Monitor

The basic configuration tab allows the user to define averaging levels, to define the source of the reference, as well as enabling external interface options. The on-chip supply monitor tab is where the sensors that monitor supply voltages and dedicated VP/VN assignments are located. For each sensor that is enabled, averaging can be enabled, and alarms can be configured. The temperature tab allows for temperature based alarm configuration. The external supply monitor tab allows for the enabling and pin assignment for the auxiliary input (AUXIO) pins. In this section, specific AUXIO pins can be assigned to package sites.

The CIPS wizard takes these user options and assigns the various enabled voltage channels to a supply number which can be assigned and identified in the CIPS configuration flow. Details on the CIPS IP be found in the *Control, Interface and Processing System LogiCORE IP Product Guide* (PG352).

IMPORTANT! *All channels that may need to be monitored are enabled in the CIPS wizard. Unlike previous architectures, debug tools, such as HW_Manager, only have access to channels configured in CIPS. There is no timing/sampling penalty for enabling many channels.*

After the channels are defined by the CIPS wizard, the PMC register map can be used to modify attributes on the defined channels. Attributes such as averaging levels and alarm thresholds can be modified through the register map in the ROOT_SYSMON module. See the *Versal ACAP Register Reference* (AM012) for SYSMON register descriptions. Software drivers are provided as part of the Vitis™ unified software platform to simplify software access to the SYSMON. Driver details can be found here.

Accessing the PMC and Processing System Considerations

The system monitor is controlled by the SYSMON_PMC register module. Software code accesses this register module to configure and control the system monitor. The registers also provide a way to read results and set interrupt alarms. Enabled interrupts can generate a system interrupts. System interrupts are routed to the PS and PMC.

In the PMC/PS, the register module is memory-mapped at base address `0xF127_0000`. This is a 32-bit APB programming interface attached to the PMC interconnect. Accesses to the register module are routed through the Xilinx peripheral protection unit for the PMC (PMC_XPPU) before reaching the system monitor. This programming interface can potentially be reached by any processor in the system, including processors instantiated in the PL.

IMPORTANT! *Access to the PMC's register module can be restricted by the PMC_XPPU. Care must be taken to configure the PMC_XPPU to ensure the necessary access to the SYSMON_PMC registers.*

A PL processor can access the register module programming interface by attaching itself to a PL-to-PS AXI interface (e.g., S_AXI_LPD). This path also requires the LPD to be powered-up.

Versal ACAP Technical Reference Manual (AM011) provides information on the PMC/PS access paths, the 4 GB address map, and system interrupts.

Considerations for Stack Silicon Interconnect Technology

When a device has multiple super logic regions (SLRs), only the voltage measurements in the master SLR's have full functionality. The SYSMON_ROOT located in the master SLR will only report voltage measurement that reside in the master SLR. As a result, I2C/PMBUS interaction is limited to reporting only voltage measurement for supplies enabled in the master SLR.

SYSMON Registers

Unlike previous generations, the SYSMON in the Versal® device does not have fixed register mapping for configuring or reading voltage results from the SYSMON. To accommodate a large variety of sensors in different devices, the SYSMON contains memory-mapped registers that are configured by the Control, Interface, and Processing IP in Vivado tools. The IP is responsible for assigning attributes and results related to a register to a specific memory location. With up to 160 channels of memory-mapped registers, the SYSMON is capable of storing results for a large variety of sensor results. All the following references to specific channel values can reference comma separated variable file (CSV) produced by the CIPS wizard to indicate which measurement source mapping.

To simplify the use of the SYSMON registers, the unified platform includes examples and API under the sysmonpsv driver. Although register names are referenced this manual, the SYSMON memory-mapped registers are described in greater detail in the SYSMON_PMC module of the *Versal ACAP Register Reference* (AM012).

Channel Registers

Each voltage channel enabled by the Control, Interface, and Processing IP provides three registers of information: Current sample captured, the maximum sample captured, and the minimum sample captured. For each voltage channel, the IP automatically assigns a mapping for a given channel number from 0 to 159. The channel number stores current conversions, minimum, and maximum conversions in the SUPPLYXX, SUPPLYXX_MIN, and SUPPLYXX_MAX registers, where XX is a fixed channel number defined by the CIPS IP. As each channel finishes a conversion or averaging cycles, the user is alerted the NEW_DATA_FLAG0 through NEW_DATA4 registers. The NEW_DATA0 through NEW_DATA4 and NEW_DATA_FLAG0 through NEW_DATA_FLAG4 indicate that a new sample is available. If no voltage channels are enabled, these registers will not update. See Chapter 3: Analog Channels for details on the format of the conversions.

For temperature, the channels DEVICE_TEMP, DEVICE_TEMP_MIN, and DEVICE_TEMP_MAX store the conversion information. The DEVICE_TEMP_MIN captures the lowest reading since reset (see STATUS_RESET) and DEVICE_TEMP_MAX captures the highest DEVICE_TEMP reading since reset (see STATUS_RESET). In addition to the DEVICE_TEMP registers, TEMP_LPD and TEMP_FPD are dedicated temperature sensors in the PS used at boot.

Alarms

Voltage alarms can be enabled through ALARM_REG0 through ALARM_REG4, with each bit in these registers representing a specific channel. As mentioned earlier, alarm lower thresholds are defined in registers SUPPLY0_TH_LOWER through SUPPLY159_TH_LOWER; while upper thresholds are defined in SUPPLY0_TH_UPPER through SUPPLY159_TH_UPPER. ALARM_FLAG0 through ALARM_FLAG4 indicate voltage alarm assertions for each of the 160 voltage based alarms in the SYSMON.

Temperature alarms are controlled by the OT_TEMP_TH_LOWER, OT_TEMP_TH_UPPER, DEVICE_TEMP_TH_LOWER, and DEVICE_TEMP_TH_UPPER registers. The ALARM_CONFIG register sets the alarm mode for the temperature sensors. Temperature alarm bits are found in the REG_ISR register.

Configuration Registers

Although the primary resource for configuring the SYSMON is through the CIPS wizard, there are some registers that can change SYSMON behavior. The CONFIG0 register in the SYSMON_PMC module allows the user to update averaging levels and configure I2C and PMBUS interfaces. The EN_AVG_REG0 through EN_AVG_REG4 registers enable voltage averaging on a per channel basis with averaging levels defined in the CONFIG0 register.

Interrupt Registers

New voltage samples are indicated through five registers, NEW_DATA_FLAG0 through NEW_DATA_FLAG4. Up to four channel interrupts can be assigned through the NEW_DATA_INT_SRC. The interrupts for both voltage and temperature results are enabled and controlled using the registers, REG_ISR, REG_IMR0, REG_IMR1, REG_IER0, REG_IER1, REG_IDR0, and REG_IDR1.

I2C or PMBus Interface

The SYSMON provides two different external command interfaces. Although I2C and PMBus modes leverage similar I2C transport structures, PMBus mode leverages the standard PMBus command interface. The SYSMON I2C and PMBus address and MIO/EMIO pin locations are configurable through the Control, Interface, and Processing IP and allows access to the SYSMON.

IMPORTANT! *I2C/PMBUS restrictions for designs that use 2.5V or 3.3V on banks 500 and 501 exist for all package and speed grade combinations of VC1902, VC1802, VM1802, VM1302, VM1402. See Versal AI Core Series Production Errata (EN313) and Versal Prime Series Production Errata (EN314) for more details.*

Several Slave Addresses are reserved by both I2C and SMBUS standards and should not be configured for I2C or PMBUS control interface. These addresses are defined in the following table. The SYSMON I2C/PMBus interfaces are not available before the SYSMON is configured. The SYSMON address can only be configured in the Control, Interface, and Processing IP.

IMPORTANT! *Neither I2C nor PMBus interfaces are active before the SYSMON is configured to enable the interface.*

Table 3: **Reserved I2C/PMBUS Slave Addresses**

Reserved Address		Standard
000 0XXX	0x00 - 0x07	I2C and SM Bus
000 1000	0x08	SM Bus
000 1001	0x09	SM Bus
000 1011	0x0B	SM Bus
000 1100	0x0C	SM Bus
010 1000	0x28	SM Bus
010 1100	0x2C	SM Bus
011 0111	0x37	SM Bus
100 00XX	0x40 - 0x43	SM Bus
100 0100	0x44	SM Bus
110 0001	0x61	SM Bus
111 1XXX	0x78 - 0x7F	I2C and SMBUS

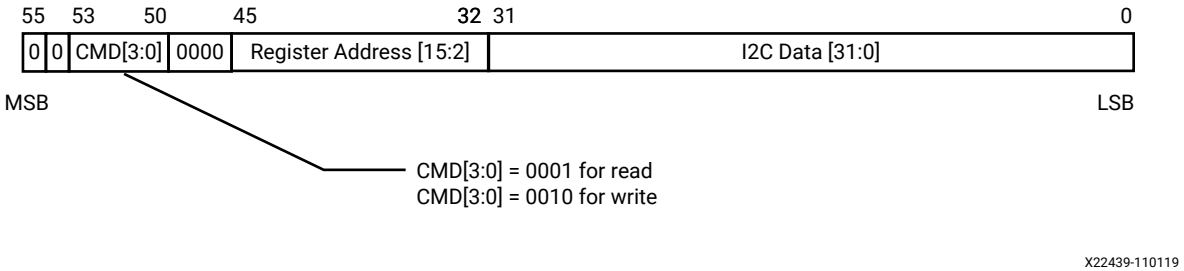
I2C Interface

The SYSMON located in the master super logic region (SLR) acts as a slave to the I2C interface. The I2C interface must be enabled and configured by the Control, Interface, and Processing IP in Vivado® tools. The SYSMON I2C slave address is user-defined through the Processor IP.

Access to the control and status registers is provided using I2C Write and Read transfers. I2C transfers data by the byte starting with the lowest byte first. Within the byte, the MSB is transferred first as shown in the following figure. I2C uses open-collector signaling, which allows bidirectional data on I2C_SDA. The following figure shows how I2C_SDA and I2C_SCLK are used to send a write to the SYSMON. The master and slave devices control the I2C interface at different times during a transfer because I2C_SDA is bidirectional. Data is transmitted eight bits at a time with an acknowledge from the receiving device every eight bits. The transfer ends with the master device terminating the transfer with a stop command.

An I2C transfer packet consists of 56 bits which define the transaction direction, the bits 15 down to 2 of the memory-mapped register relative address being accessed, and a 32-bit data portion. A SYSMON I2C command has the structure shown in the following figure.

Figure 14: **56-bit I2C Command Format**



I2C Transfers

The following figures illustrate a SYSMON I2C Write and a SYSMON I2C Read.

I2C_Read and I2C_Write

Figure 15: **I2C Write Instruction Example**

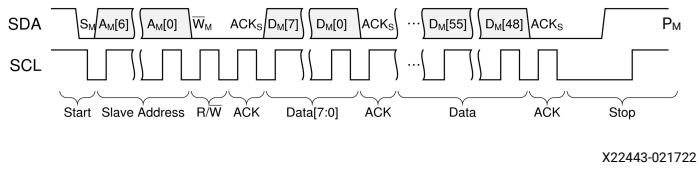


Figure 16: **I2C Read Instruction Example**

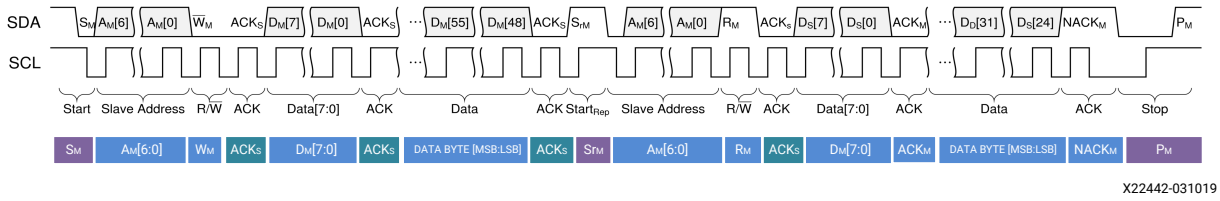


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Table 4: **Command Description**

Command	Description
S_M or Sr_M	Start or repeated start (there is no stop before repeated start) - master to slave
$A_M[6:0]$	7-bit slave address – master to slave
ACK_S	0, acknowledgment – slave to master
ACK_M	0, acknowledgment – master to slave
$NACK_M$	1, not acknowledgment – master to slave
D_M	See the previous figure for 56-bit I2C command format sent 8 bits at a time
D_S	32-bit command response sent 8 bits at a time
P_M	Stop – master to slave

PMBus Interface

For applications supporting the PMBus power system protocol specification, the SYSMON adds the SMBALERT output as described in the PMBus specification. This optional pin provides an interrupt output and supports alert response address (ARA) functionality as defined by the PMBus specification.

IMPORTANT! *The SMBALERT continues to be asserted while the failing condition exists.*

PMBus Transfer Commands

Table 5: **PMBus Transfer Commands**

Code	Command	Description	Transaction Type	Local Register Name	Data Bytes (Format)	Scope
00h	PAGE	Selects the supply for the single supply commands (Scope = PAGE).	Read Write	PMBUS_PAGE	1	COMMON

Table 5: **PMBus Transfer Commands** *(cont'd)*

Code	Command	Description	Transaction Type	Local Register Name	Data Bytes (Format)	Scope
03h	CLEAR_FAULTS	Clears all fault bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBALERT# signal output if the device is asserting the SMBALERT.	Write	ALL PMBUS STATUS REG	0	COMMON
19h	CAPABILITY	Allows host to identify key capabilities of PMBus device, i.e., PEC support, max bus speed, SMBALERT support. Returns 0x30.	Read		1	COMMON
20h	VOUT_MODE	To set and query the data format used by device for output voltage related data.	Read Write		1	COMMON
40h	VOUT_OV_FAULT_LIMIT	Sets the over-voltage value that causes an output over-voltage fault.	Read Write	Upper threshold register for the supply addressed by PAGE setting.	2 (LINEAR16)	COMMON
44h	VOUT_UV_FAULT_LIMIT	Sets the under-voltage value that causes an output over-voltage fault.	Read Write	Lower threshold register for the supply addressed by PAGE setting.	2 (LINEAR16)	COMMON
4Fh	OT_FAULT_LIMIT	Command sets the temperature of the unit at which it should indicate an over temperature fault OT	Read Write		2 (LINEAR11)	COMMON
51h	OT_WARNING_LIMIT	Command sets the temperature of the unit at which it should indicate an over temperature warning ALM_OV[0].	Read Write		2 (LINEAR11)	COMMON
52h	UT_WARNING_LIMIT	Command sets the temperature of the unit at which it should indicate an under temperature warning ALM_UV[0].	Read Write		2 (LINEAR11)	COMMON
53h	UT_FAULT_LIMIT	Command sets the temperature of the unit at which it should indicate an under temperature fault UT.	Read Write		2 (LINEAR11)	COMMON
78h	STATUS_BYTE	Command returns one byte of information with a summary of the most critical faults.	Read		1	COMMON

Table 5: **PMBus Transfer Commands** *(cont'd)*

Code	Command	Description	Transaction Type	Local Register Name	Data Bytes (Format)	Scope
79h	STATUS_WORD	Command returns two bytes of information with a summary of the unit's fault condition.	Read		2	COMMON
7Ah	STATUS_VOUT	Command returns one byte representing VOUT status.	Read Write		1	PAGE
7Dh	STATUS_TEMPERATURE	Command returns temperature status.	Read Write		1	COMMON
7Eh	STATUS_CML	Command returns communication, logic, and memory status.	Read Write		1	COMMON
8Bh	READ_VOUT	Command returns the actual, measured (not commanded) output voltage in the LINEAR16 format.	Read		2 (LINEAR16)	PAGE
8Dh	READ_TEMPERATURE_1	Command returns temperature readings.	Read		2 (LINEAR11)	COMMON
98h	PMBUS_REVISION	PMBUS_REVISION command stores or reads the revision of the PMBus to which the device is compliant.	Read		1	COMMON
99h	MFR_ID	PMBUS_REVISION command reads the Xilinx manufacturer's ID.	Read		3	COMMON
9Ah	MFR_MODEL	The command is used to read the manufacturer's model number of the part.	Read		3	COMMON
9Bh	MFR_REVISION	The command is used to either set or read the manufacturer's revision number.	Read		2	COMMON
D0h	MFR_SPECIFIC_D0	(MFR_SELECT_REG) A manufacturer-specific command to program config and sequence registers. The command is used to select memory-mapped registers.	Read Write		2	COMMON
D1h	MFR_SPECIFIC_D1	(MFR_ACCESS_REG) Read or write data on the selected register.	Read Write		4	COMMON
D2h	MFR_SPECIFIC_D2	(MFR_READ_VOUT_MAX) A manufacturer-specific command. Reads maximum recorded value for the selected supply.	Read		2 (SLINEAR16)	PAGE

Table 5: **PMBus Transfer Commands** *(cont'd)*

Code	Command	Description	Transaction Type	Local Register Name	Data Bytes (Format)	Scope
D3h	MFR_SPECIFIC_D3	(MFR_READ_VOUT_MIN) A manufacturer-specific command. Reads minimum recorded value for the selected supply.	Read		2 (SLINEAR16)	PAGE
D4h	MFR_SPECIFIC_D4	(MFR_VOUT_OV_FAULT_LIMIT) Command sets the value of the output voltage measured at the sensor that causes an output over-voltage fault.	Read Write		2 (SLINEAR16)	PAGE
D5h	MFR_SPECIFIC_D5	(MFR_VOUT_UV_FAULT_LIMIT) Command sets the value of the output voltage at the sensor or output pins that cause an output under-voltage fault.	Read Write		2 (SLINEAR16)	PAGE
D6h	MFR_SPECIFIC_D6	(MFR_READ_TEMP_MAX) A manufacturer-specific command. Reads max recorded value for the device temperature.	Read		2 (LINEAR11)	PAGE
D7h	MFR_SPECIFIC_D7	(MFR_READ_TEMP_MIN) A manufacturer-specific command. Reads the minimum recorded value for the device temperature.	Read		2 (LINEAR11)	PAGE
D8h	MFR_SPECIFIC_D8	(MFR_RESET_TEMP) Command resets the minimum and maximum recorded device temperatures.	Write		0	COMMON
D9h	MFR_SPECIFIC_9	(MFR_READ_VOUT) Command returns the actual, measured (not commanded) output voltage in the SLINEAR16 format.	Read		2 (SLINEAR16)	PAGE
DAh	MFR_RESET_SUPPLY	(MFR_RESET_SUPPLY) Command resets the minimum and maximum recorded voltages for all supplies.	Write		0	COMMON

Command Description

Table 6: **Command Description**

Command	Description
S_M or Sr_M	Start or repeated start (there is no stop before repeated start) – master to slave
A_M[6:0]	7-bit slave address – master to slave
CMD_M[7:0]	8-bit PMBus command code
ACK_S	0, acknowledgment – slave to master
ACK_M	0, acknowledgment – master to slave
$NACK_M$	1, not acknowledgment – master to slave
D[7:0] or D[15:0]	Logical register/SYSMON register address
P_M	Stop – master to slave

PMBus Data Formats

The SYSMON supports different data formats depending on commands. LINEAR16 format commands are for voltages using the PMBus format. LINEAR11 format commands are for temperatures using the PMBus format and one- to four-byte transfers. This section explains how the different data formats should be used for the SYSMON.

LINEAR16 Format

LINEAR16 is based on 16-bit unsigned value as described in the following equation.

$$\text{LINEAR16} = \text{M} \times 2^{-14}$$

For example, to set VOUT_OV_FAULT_LIMIT to 0.979V, 3EA8h is written for command 40h. From the following table, high byte = 3E and low byte = A8h. To set VOUT_UV_FAULT_LIMIT to 0.922V, 3B02h is set to command 44h.

Table 7: **LINEAR16 Data**

High Byte								Low Byte							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M (16-bit, unsigned)															

SLINEAR16

SLINEAR16 is based on 16-bit signed value as described in the following equation.

$$\text{SLINEAR16} = \text{M} \times 2^{-15}$$

Table 8: **SLINEAR16 Data**

High Byte								Low Byte							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M (16-bit, signed)															

The 8-bit data contains the 3-bit mode setting, `000b` for linear, and a 5-bit exponent setting as shown in the following table. The three mode bits must always be `000b`, and the 5-bit exponent is -14 for LINEAR16 and -15 for SLINEAR16.

Table 9: **VOUT_MODE Data Byte for LINEAR16 (Code 20h)**

Mode (linear)			Exponent (-14)				
7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0

Linear11 Format

For temperature values for PMBus commands, the SYSMON uses the following equation.

$$\text{LINEAR11} = \text{M} \times 2^{\text{N}}$$

For LINEAR11, M is an 11-bit, twos complement value as shown in the following table. N is a 5-bit, twos complement exponential value. For example, N = 00h and M = 50h (with a resulting 16-bit register value of 0050h) is used to set the temperature to 80°C. N = 00h and M = 7ECh (with a resulting 16-bit register value of 07ECh) is used to set the temperature for –20°C. To set the temperature to 80.125°C, set N = 1Dh and M = 281h (with a resulting 16-bit register value of EA81h).

Table 10: **Linear11 Data**

High Byte								Low Byte							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N (5-bit, twos complement)					M (11-bit, twos complement)										

PMBus Example

The following diagram illustrates a typical PMBus command.

Figure 17: **Typical PMBus Command**

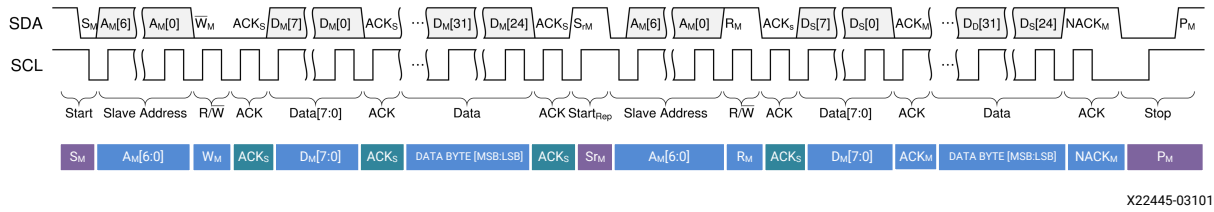

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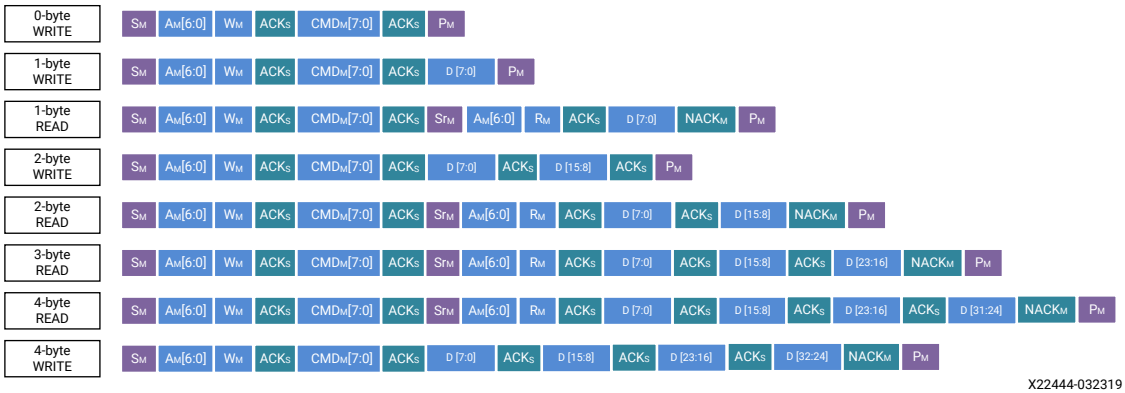
Table 11: **SYSMON PMBus Label Descriptions**

Command	Description
S_M	Start command - master to slave
$A_M[6:0]$	7-bit I2C slave address - master to slave
R/W_M	Read (1) / Write (0) command - master to slave
ACK_S	Acknowledge - slave to master
$D_M[7:0]$, DATA BYTE[MSB:LSB]	56-bit SYSMON write command sent in bytes separated by ACKs
Sr_M	Repeated start command - master to slave
$D_S[7:0]$, DATA BYTE[MSB:LSB]	32-bit SYSMON read data sent in bytes separated by ACK_M
ACK_M	Acknowledge - master to slave
$NACK_M$	Not acknowledge - master to slave
P_M	Stop command - master to slave

Many PMBus commands require multiple byte read and write commands. The following diagram illustrates a general overview of the various sized commands supported by SYSMON.

Figure 18: **Command Sequences**



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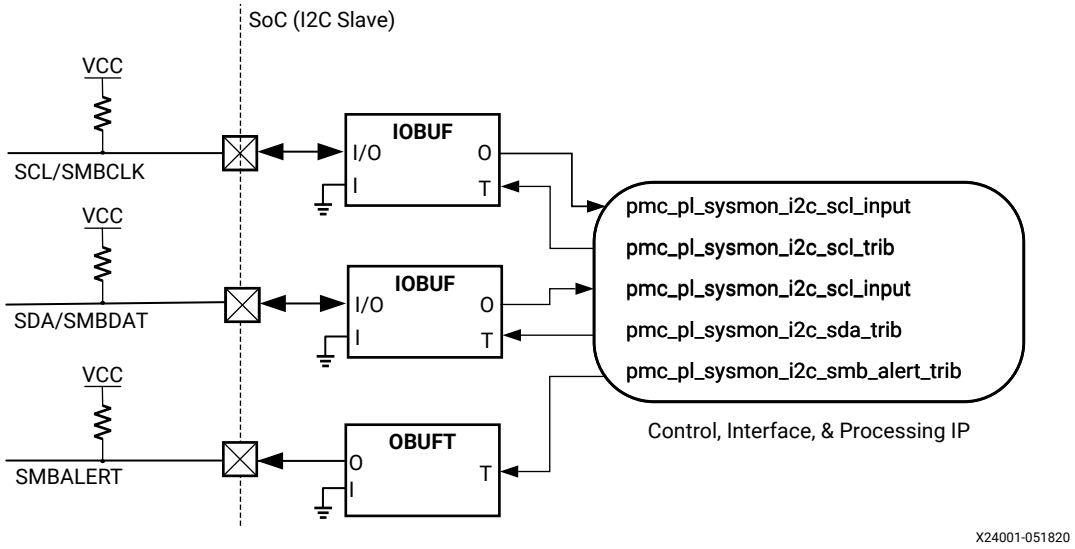
Connecting I2C or PMBUS through SelectIO (PL) Package Pins

In the CIPS wizard, MIO or EMIO ports can be selected for I2C or PMBUS port assignments. CIPS automatically handles the connection of MIO pins and provides ports to the IP instance when the I2C or PMBUS interface is desired to connected through SelectIO pins in the PL portion of the device.

As shown in the following figure, two bidirectional package pins are required for the I2C while PMBUS has an additional output pin (SMBALERT). The SMBALERT pin provides an interrupt output and supports alert response address (ARA) functionality as defined by the PMBUS specification.

Figure 19: **Connecting I2C/PMBUS to SelectIO Package Pins**



AMD XILINX

Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

***Note*:** For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. *Versal ACAP Register Reference* (AM012)
2. *XADC Layout Guidelines* (XAPP554)
3. *Driving the Xilinx Analog-to-Digital Converter* (XAPP795)
4. Versal ACAP data sheets
   - *Versal Architecture and Product Data Sheet: Overview* (DS950)
   - *Versal Prime Series Data Sheet: DC and AC Switching Characteristics* (DS956)
   - *Versal AI Core Series Data Sheet: DC and AC Switching Characteristics* (DS957)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
05/17/2022 Version 1.3	
SYSMON Architecture	Added note about SLR.
Temperature Sensor	Updated to address temperature variation. Added reference.
Averaging	Updated temperature sensor voltage averaging.
Analog Power Supply and Ground	Removed additional regulator recommendation.
Analog Input Description	Removed additional regulator recommendation.
Configuring the SYSMON	Updated information on CIPS configuration flow.
Chapter 7: I2C or PMBus Interface	Added table to address reserved I2C/PMBus slave addresses. Added references.
04/19/2021 Version 1.2	
SYSMON Dedicated Pinout Requirements	Updated to indicate that V_{CCAUX_SMON} must be tied to the V_{CCAUX_PMC} supply.
Over-Temperature Shutdown	Updated to clarify PMC behavior.
I2C Interface	Clarified description.
12/04/2020 Version 1.1	
SYSMON Architecture	Updated PMC main switch description as well as updated the figure to remove DXP/DXN ports.
SYSMON Supply and Reference Requirements	Updated recommendation to use internal reference.
SYSMON Dedicated Pinout Requirements	Updated package pinout names.
Differences from Previous Generations	Added information about improved noise immunity.
Chapter 3: Analog Channels	Added details about CIPS behavior.
Supply Sensors	Added a note about IR drop consideration.
Bank Ground	Added information on how to enable bank GND.
External Multiplexer Functionality	Removed section.

Section	Revision Summary
Averaging	Added a reference to averaging control register, as well as added a note to explicitly call out shared averaging levels.
Maximum/Minimum Tracking	Updated description.
Alarms	Added register details and information about alarm behavior.
Over-Temperature Shutdown	Added references to registers.
Analog Power Supply and Ground	Updated to recommend the use of on-chip reference.
Analog Input Description	Clarified description.
Configuring the SYSMON	Added details about using the CIPS wizard.
Accessing the PMC and Processing System Considerations	Added section.
Chapter 6: SYSMON Registers	Added information about interrupts as well as other SYSMON registers.
07/16/2020 Version 1.0	
Initial release.	N/A

Please Read: Important Legal Notices

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