AMD PCB Channel Design Guidelines for 112 Gbps GTM Transceivers

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Summary

High-speed data rate transmissions suffer from distortions to the signal imposed by channel response. 112 Gbps continues to push channel design considerations, both at the board level and in the transceiver. The small unit interval of the symbol combined with the reduced eye amplitude of the 4-level pulse amplitude modulation (PAM4) scheme results in less available budget for impairments, such as crosstalk and jitter. This application note details printed circuit board (PCB) channel design requirements for high-speed serial data transmission, including rates of 56 Gbps and 112 Gbps. Good practices for minimizing and mitigating the various impairments on the PCB are also presented.

Download the reference design files for this application note from the Versal ACAP Transceiver IBIS-AMI Model Secure website. For detailed information about the design files, see Reference Design.

Introduction

When data rates approach 56 Gbps per lane, a more bandwidth-efficient modulation scheme (PAM4) is deployed. However, PAM4 signaling is susceptible to noise, including intersymbol interference (ISI) and crosstalk, because the eye height is reduced while still generating full amplitude signal swings. The result is the potential worst-case condition of the signal aggressor having a full height voltage transition, while the victim simultaneously has a swing of 1/3 the full height.

As shown in the following figure, taken from Overview of ADC-based Wireline Transceiver [1], suppose the designed channel has 10% reflection at the fifth cursor *h5*, the amplitude of *Bit 5* (green waveform) is h (minor transition from 1/3 to -1/3). For a major transition *Bit 0* (from -1 to 1) with amplitude of $3 \times h$ occurs at cursor *h0* (red waveform), the amplitude of the reflected signal at the fifth cursor *h5* is $0.3 \times h (10\% \times 3 \times h)$, which is 30% of *Bit 5*'s amplitude h. The impact of the residual ISI on PAM4 is three times its non-return-to-zero (NRZ) counterpart.



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Figure 1: PAM4 Challenges



As data rates increase further to 112 Gbps, the unit interval is less than 20 picoseconds. Large numbers of DFE or FFE taps at the RX side are required to manage the multiple reflections from discontinuities that show up far away from the main cursor. A *Tutorial on PAM4 Signaling for 56G Serial Link Applications* [2] provides a thorough review of PAM4 signaling.

The small unit interval combined with PAM4 modulation reduces channel design budget to the point where each element in the channel matters. Besides meeting the channel insertion loss budget, dedicated design efforts should be taken to minimize impedance discontinuity, crosstalk, and skew on the channel.

High-speed data rate transmissions suffer from distortions to the signal imposed by channel response. The most significant impairments from the passive channel include:

- Frequency-dependent attenuation and dispersion from conductor loss and dielectric loss lead to insertion loss (IL).
- Reflections/multiple reflections from discontinuities and impedance mismatch lead to return loss/effective return loss (RL/ERL).
- Crosstalk due to unwanted horizontal coupling and vertical coupling lead to power sum crosstalk (PSXT), insertion loss to crosstalk ratios (ICR), and integrated crosstalk noise (ICN).
- Intra-pair skews originating from asymmetry structure, glass weave, and trace length mismatch lead to mode conversion (SDC/SCD).

The GTM transceiver in the AMD Versal[™] adaptive SoC is a dual-mode, multi-protocol transceiver supporting multiple electrical standards, including OIF CEI-56G-VSR/MR/LR [3], and IEEE 802.3bs/cd/ck [4]. It addresses both in-box and out-of-box interconnects, from short reach to long reach (LR) chip-to-chip interfaces within the PCB and across the PCB through board-to-board connecters or direct attached cables (DAC), optical interfaces through pluggable optical modules, or the emerging technology of on-board optics/near-package optics [5].

This application note details the requirements and good practices for minimizing and mitigating various impairments and achieving successful 112 Gbps high-speed serial link designs. These requirements are provided with the channel requirements of any supported protocol. Supported protocols are listed in the datasheets for the Versal devices with GTM transceivers.

• Versal Prime Series Data Sheet: DC and AC Switching Characteristics (DS956)





- Versal Premium Series Data Sheet: DC and AC Switching Characteristics (DS959)
- Versal HBM Series Data Sheet: DC and AC Switching Characteristics (DS960)

Channel Insertion Loss

One ultimate challenge for 112 Gbps electrical interfaces is achieving the desired physical reach while still meeting the constraints of power consumption and bandwidth-limited channels. High-speed data rate transmissions suffer from the frequency-dependent attenuation and dispersion induced by PCB-based or electrical cable-based interconnects.

As illustrated in the following figure, frequency-dependent attenuation and dispersion arise from frequency-dependent conductor loss and dielectric loss, where conductor loss can be subdivided into smooth copper loss due to skin effects and additional loss due to a rough conductor surface. While the die bump-to-die bump channel insertion loss budget is around 35 dB for long reach applications in each generation from 25 Gbps to 100 Gbps, low-loss PCB material, smoother copper with advanced surface treatments, and/or wider traces are required to fulfill the IL budget in the 100 Gbps era.



Figure 2: PCB Material Loss Decomposition



The designed channel must meet the recommended maximum and minimum channel insertion loss stipulated in corresponding electrical standards. When paired with a long reach-capable transceiver, the Versal device GTM transceiver can support up to 30 dB ball-to-ball loss (refer to the corresponding standards for the maximum channel IL budgets) at Nyquist (14 GHz for 56 Gbps PAM4 or 28 GHz for 112 Gbps PAM4) with Reed-Solomon (544, 514) Forward Error Correction (RS (544, 514) FEC).

The maximum IL a Versal device GTM transceiver can support also depends on the channel characteristics like discontinues and crosstalk. The designed channel should be evaluated with the channel compliance methods stipulated in the corresponding standard to verify the conformance.

IMPORTANT! The recommended channel insertion loss requirement (Nyquist = 14 GHz / 28 GHz) is as follows:

PCB differential insertion loss (@ ≤ Nyquist) from ball-to-ball: ≤ 30 dB

- Insertion loss deviation range 1 [@ ≤ Nyquist]: ≤ ±0.5 dB
- Insertion loss deviation range 2 [@ Nyquist ≤ F ≤ (1.5 x Nyquist)]: ≤ ±1.0 dB

Impedance Discontinuity

Impedance discontinuity causes energy reflection. With the presence of an impedance discontinuity in the transmission path, part of the transmitted signal reflects back to the transmitter and is not detected by the receiver. Each discontinuity reduces the amount of signal that is delivered to the receiver. In addition, multiple reflections distort the forward propagating waveform. Common sources of discontinuities include package-to-PCB interfaces, PCB vias, surface-mount device (SMD) footprints, connectors, and cable-to-connector interfaces.

Via Impedance Optimization

- PCB vias are a source of impedance discontinuities if not properly designed. The via stub, antipad size, drill hole size, and differential via pitch are important features for via impedance control.
- Minimizing via stub is crucial for securing 112 Gbps channel designs. A via stub can cause a ¹/₄ wave resonance. At the resonance frequency, a deep notch appears on the insertion loss due to the cancellation between the 180-degree out-of-phased reflected signal from the stub and the transmitting signal. The resonance frequency can be estimated as follows.

Equation 1: 1/4 Wave Resonance Frequency

$$f_{res} = \frac{c}{4 \times l \times \sqrt{Dk_{eff}}}$$

Where f_{res} is the ¼ wave resonance frequency, *c* is the speed of light in vacuum, *l* is the stub length, and Dk_{eff} is the effective dielectric constant the via sees. Dk_{eff} is normally higher than the PCB dielectric material's dielectric constant because of the coupling between via barrel/ pads and the reference planes surrounding the via. To minimize the impact of the ¼ wave resonance on the signal, it is recommended to push the resonance frequency well above the signal bandwidth, for example, > 2 × signal bandwidth.





- The most common way to match via impedance with channel nominal impedance is tuning the via antipad size to adjust the capacitance and inductance ratio. However, a small via antipad is preferred in the ball grid array (BGA) pin field to reduce the trace-via crosstalk. For the BGA via impedance optimization, return loss and crosstalk should be evaluated simultaneously to determine the optimal point for maximal system margin.
- For the blind via, extending the antipad void to the layers beneath the via mitigates the excess capacitance from the coupling between the via pad and the planes. For a blind via with a lead-out trace not routed on the bottom layer of the via, for example a blind via in sequential lamination, removing the via bottom layer pad like a landless via helps with minimizing the capacitance as well, as shown in the following figure.

Figure 3: Landless Blind Via

- Unlike the 25 Gbps NRZ / 56 Gbps PAM4 channel where an identical antipad on all the layers is sufficient for optimal via impedances in the frequency band of interest, tuning the antipad size/shape per layer is necessary to keep a low return loss for the wider frequency band in 112 Gbps designs.
 - The antipad voids on the stripline reference plane layers have a significant impact because of the excess inductance from the lead-in/out trace losing its reference in the void range.
 - The antipad void on layer 2 has a significant impact because of capacitive coupling to the top layer pad.
- Spacing of the signal and GND vias has a significant impact. Outside the BGA pin field, the GND vias should be placed as close to the signal via as possible, but not encroach into the signal via antipad void range. In the BGA pin field, the placement of GND vias should follow the pattern of GND balls.

SMD Footprint Optimization

• Another significant discontinuity on the link is the footprint of the SMD, such as AC coupling capacitors, board-to-board connectors, and BGA pads.



- Generally, the footprints show excess capacitance with the combination of dielectric thickness to the reference plane and footprint geometries. Thus, the reference plane beneath the SMD pads should be voided to remove the capacitance.
- Both an optimal cut-out depth and cut-out size (width, length, and radius) that minimize the return loss of the structure should be identified.

Optimal Channel Nominal Impedance

- When there are large discontinuities that cannot be eliminated, the optimal trace impedance should be determined in a way that minimizes the multiple reflections from the discontinuities. It is not necessary to adhere to 100Ω or 85Ω.
- The nominal trace impedance of the Versal device GTM transceiver channel package is 92 \sim 93 Ω \pm 10%.

Figure 4: Discontinuity Examples

• The channel nominal impedance should be selected per system-level SI analysis with all discontinuities included.



Via & AC coupling capacitor footprint



Connector footprint and mating interface



As illustrated in the previous figure, discontinuities usually occur at vertical transition regions, like package-to-PCB interfaces and PCB-to-connector interfaces. Attention to detail at every signal transition region is critical to achieve a successful 112G channel design.

IMPORTANT! The recommended channel return loss requirement is as follows:

- PCB differential return loss (@ ≤ Nyquist): ≤ -12 dB [at the solder ball]
- PCB common-mode return loss (@ ≤ Nyquist): ≤ -15 dB



- PCB differential-to-common mode return loss (@ all frequencies): ≤ -15 dB
- PCB common-to-differential mode return loss (@ all frequencies): ≤ -15 dB

Crosstalk

Crosstalk is unwanted coupling between aggressor signals and victim signals, which can happen anywhere throughout the link. Common sources of crosstalk are connectors, BGA vias, PCB/ package traces, cables, AC coupling capacitors and accompanying vias. In all cases, crosstalk is a function of the relative signal strength of the aggressor versus the victim at the region of coupling. For instance, if the victim is a receive channel that has incurred 30 dB of attenuation, and the aggressor is a nearby transmitter that has yet to encounter any attenuation, the crosstalk isolation must account for the strength of the aggressor. In this example, if the aggressor is 30 dB stronger than the victim, the crosstalk isolation must include at least 30 dB of isolation to counteract the aggressor signal strength. Because crosstalk is dependent on the relative strength of the victim and the aggressor, crosstalk isolation is especially important when adjacent channels have very different insertion loss profiles.



Figure 5: Crosstalk Examples

IMPORTANT! The recommended channel crosstalk requirement is as follows:

- Worst-case signal to power sum crosstalk ratio (IL roll-off with frequency, crosstalk flat or rampup with frequency) up to Nyquist frequency for NRZ application ≥ 20 dB
- Worst-case signal to power sum crosstalk ratio up to Nyquist frequency for PAM4 application ≥ 30 dB due to ~10 dB signal-to-noise ratio (SNR) lost by splitting one eye in NRZ into three in PAM4 (aggressor full swing victim 1/3 full swing)

As illustrated in the following figure, within the BGA pin field there are three types of crosstalk:

• **TX-TX Coupling:** This type of coupling is not influenced by the channel loss because the signal has yet to encounter the channel. Therefore, the crosstalk isolation required is independent of the channel loss for either the victim or aggressor.



- **RX-RX Coupling:** An important factor in calculating the required crosstalk isolation is the relative insertion loss of the victim and aggressor channels. If the victim channel is an LR channel with 30 dB of insertion loss and the aggressor is a short reach channel with only 10 dB of insertion loss, the crosstalk isolation must include attenuation of 20 dB to account for the difference between the aggressor and victim signal strength. Because of this, it is important to identify cases in the application where there is a disparity between the insertion loss of the victim and the aggressor.
- **TX-RX Coupling:** The TX incurs little attenuation while the attenuation of the RX can vary significantly. This type of crosstalk coupling is very dependent on insertion loss in the RX channel and is independent of the channel loss in the TX channel. The greater the loss in the RX channel, the more crosstalk isolation is required between the TX and RX. This coupling does not depend on the type of channel like LR and very short reach (VSR) for TX as is the case for TX-TX coupling. Instead, it is completely dependent on the RX channel insertion loss. More channel insertion loss requires more crosstalk isolation.



Figure 6: Crosstalk Components

The crosstalk isolation requirement is a function of the assigned crosstalk allowed in the channel link impairment budget, the victim, and the relative strength of the victim and the aggressor. For NRZ signaling, the type of coupling is used to define the relative strength of the victim and the aggressor. For PAM4 signaling, an additional 10 dB of isolation is required to cover the case when the aggressor signal swing is full amplitude and the victim swing is only 1/3 of that amplitude. So, for PAM4 signaling, if the budget for the crosstalk component is 10%, the crosstalk isolation for all types of coupling would be 30 dB. The isolation due to the type of coupling, TX-TX, RX-RX, or TX-RX, is added. See the following table for examples of crosstalk targets for various interface boundary conditions.

Protocol Interface Boundary	Vict Inse Lo	tim ³ rtion ss	Aggre Inse Lo	essor ³ rtion oss	Budget ¹ (dB)	PAM4 ² (dB)	Minimum Isolation Target Power Sum for PAM4 ⁴ (dB)			Minimum Isolation Target Power Sum for NRZ ⁵ (dB)		
Boundary	RX (dB)	TX (dB)	RX (dB)	TX (dB)			RX- RX	TX- RX	TX- TX	RX- RX	TX- RX	TX- TX
VSR-LR	35	5	10	0	20	10	55	65	35	45	55	25
VSR-VSR	15	5	5	0	20	10	40	45	35	30	35	25

Table 1: Examples of Isolation Targets for Various Interface Boundary Conditions





Table 1: **Examples of Isolation Targets for Various Interface Boundary Conditions** *(cont'd)*

Protocol Interface Boundary	Vict Inse Lo	tim ³ rtion oss	Aggre Inse Lo	essor ³ rtion oss	Budget ¹ PAM4 ² (dB) (dB)	Minimum Isolation Target Power Sum for PAM4 ⁴ (dB)			Minimum Isolation Target Power Sum for NRZ ⁵ (dB)			
Boundary	RX (dB)	TX (dB)	RX (dB)	TX (dB)			RX- RX	TX- RX	TX- TX	RX- RX	TX- RX	TX- TX
LR-LR	35	5	23	0	20	10	42	65	35	32	55	25

Notes:

- 1. Allow 10% of eye for crosstalk component.
- 2. Reduce eye to one third of full signal swing for PAM4 signaling.
- 3. Loss applied to signal for signal amplitude at BGA ball.
- 4. Min Isolation Target for PAM4 = Budget + PAM4 + VictimIL Aggressor IL.
- 5. Min Isolation Target for NRZ = Budget + Victim IL Aggressor IL.

The reason that the BGA pin field is usually a high crosstalk region is the via-via and trace-via coupling. The breakout layer should be assigned in a way that minimizes the via-via and trace-via coupling. Some good practices for minimizing the crosstalk in a BGA pin field are as follows:

- A shallow breakout layer with a short via barrel and thus small vertical parallelism is preferred to minimize via-via coupling.
- If a long via barrel must be used, staggering the routing layers of adjacent pairs is a good practice to reduce via vertical parallelism.
- Route inner pairs on lower layers rather than outer pairs to avoid trace-via coupling.
- Place GND vias along the BGA field edge to improve isolation for pairs at the edge of the ball array.

IMPORTANT! The recommended channel crosstalk requirement for the BGA PCB breakout region for PAM4 signaling is as follows:

- Worst-case differential TX power sum of all aggressors to victim TX: < -35 dB up to Nyquist frequency
- Worst-case differential RX power sum of all aggressors to victim RX: < -55 dB up to Nyquist frequency
- Worst-case differential TX power sum of all aggressors to victim RX: < -65 dB up to Nyquist frequency

Intra-pair Skew

The skew between the two legs of a differential pair causes differential signal to common mode signal conversion as well as reverse mode conversion. Mode conversion distorts the differential signal and thus creates a reduced differential signal. A common mode signal might re-convert back into a differential signal, creating increased differential noise. Some common sources of skew are asymmetrical structures from manufacturing variations or unintentional return path asymmetry, glass weave, and trace length mismatch. In *Sources and Compensation of Skew in Single-Ended and Differential Interconnects* [9], you will find a review of various sources of intrapair skews.



Intra-pair Trace Length Matching

- The differential signal and common mode signal in a microstrip or via have different propagation velocities due to the different effective dielectric constants of the surrounding materials seen by the signals.
- The propagation velocities of the differential signal and common mode signal differ in an inhomogeneous stripline because the core and pre-preg around the signal conductors have different dielectric constants and loss tangents. There are also different spatial distributions of resin and glass weave around the signal/GND conductors.
- Due to the different propagation velocity for the two modes, the skew on a microstrip should be compensated just after where the skew occurs, similar to an inhomogeneous stripine. Eliminating length compensation by routing bend/turning with arcs is preferred rather than compensating the skew with a single big loop or several small serpentines.
- Similarly, due to the different propagation velocity in a via, the skew should be compensated before a trace enters the via, even if both ends of the via are stripline with a similar dielectric constant. That is, the skew compensation should be made on the same layer as where the skew occurs.
- The skew on a homogeneous stripline can be compensated with reversed (mirrored) bends, a single big loop, or several small serpentines. When compensating skew with serpentines, maintain sufficient spacing between adjacent legs to avoid self-coupling between the segments. The goal is to maintain the impedance and validate the compensation structure with simulation.

One significant contributor to mode conversion is glass weave skew. Resin and woven glass fibers have different electrical properties in terms of dielectric constants and loss tangents. When one leg of a differential pair is routed on resin and the other is routed on glass fiber, skew is generated due to different propagation velocities. There has been significant industry research in this area that characterizes the impact of glass weave and identifies methods to mitigate its effect [10, 11, and 12]. Some commonly used methods to mitigate the weave skew effect are listed below. Appropriate methods should be picked based on the balance between cost and implementation effort to minimize the glass weave skew effect.

- Angled or zig-zag routing
- Jagged routing per differential pair pitch
- Rotating the panel
- Matching differential pair pitch to weave pitch
- Multi-ply with different weave pitches
- Advanced weave, for example, glass fiber with low dielectric constant (closer to the resin dielectric constant), tighter weave



Figure 7: Intra-pair Skew Examples



System-Level SI Analysis

The Versal device GTM transceiver is designed and validated to meet protocols that assume the passive channel and link partner are compliant in all cases. The designed channel must be evaluated with a channel compliance tool or tolerancing test method stipulated in corresponding standards like channel operation margin (COM) for IEEE and OIF CEI to verify the conformance. In addition to channel compliance checks, channel simulation using an IBIS algorithmic modeling interface (IBIS-AMI) model should be run to confirm the final system margin.



Figure 8: End-to-End Channel Model





Figure 9: Channel Compliance Checking with COM







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Guidance for C4072 Package PCB Breakout

As mentioned in the Crosstalk section, a BGA pin field is a high crosstalk region due to via-via and trace-via coupling from the limited routing space. This section details important design considerations for the VP1802 C4072 package PCB breakout. These considerations should be carefully studied when using full Versal device GTM transceiver Quads for 56 Gbps LR-LR and VSR-LR reach applications. When using half of the channels in each of the Versal device GTM transceiver Quads, 112 G LR-LR operation is achievable by following the same design considerations. For designs that exceed these guidelines, consider using the A5601 package instead which supports 56 Gbps full-density Versal device GTM transceiver Quad implementation from VSR to LR reaches. See Versal Adaptive SoC Packaging and Pinouts Architecture Manual (AM013) for the design considerations regarding the A5601 package.

C4072 BGA Pin Pattern Examples

The BGA pin pattern examples for 56 Gbps full-density Quad usage are illustrated in the following figure. As shown in the figure, the RX pairs are located along the periphery of the BGA. TX pairs are located at the interior with one column of GND balls for TX-to-RX isolation. The worst-case victim RX/TX pair is surrounded by four diagonal aggressors plus two non-diagonal aggressors separated by a pair of GND balls. In addition to the RX-to-RX/TX-to-TX crosstalk, the trace-via coupling due to the TX pair lead-out traces routed near the RX pair via barrels can jeopardize the TX-to-RX isolation.

		GND	GND	RX to	RX	
GND	GND	RXP3 207	RXN3 207	GND	GND	PCB GND VIA
RXP2 207	RXN2 207	GND	GND	RXP1 207	RXN1 207	PCB GND VIA
GND	GND	' XP0 207	RXN0 207	GND	GND	PCB GND VIA
RXP3 206	RXN3 206	GND	GND	RXP2 206	RXN2 206	PCB GND VIA
GND	GND	RXP1 206	RXN1 206	GND	GND	PCB GND VIA
		GND	GND			

Fiaure	11:	BGA	Pin	Pattern	Examples -	56	Gbps	Ouad
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	TX to TX			GND			GND
GND	GND	GND	TXP3 207	TXN3 207	GND	GND	GND
GND	TXP2 207	TXN2 207	GND	GND	TXP1 207	TXN1 207	GND
GND	GND	GND	TXP0 207	TXN0 207	GND	GND	GND
GND	TXP3 206	TXN3 206 —	GND	GND	TXP2 206	TXN2 206	GND
GND	GND	GND	TXP1 206	TXN1 206	GND	GND	GND
			GND	GND			

GND	TX to	TX to RX		GND	GND
TXN3 207	GND	GND	GND	RXP2 207	RXN2 207
GND	TXP1 207	TXN1 207	GND	GND	GND
TXN0 207 —	GND	GND	GND	RXP3 206	RXN3 206
GND	TXP2 206	TXN2 206	GND	GND	GND
TXN1 206	GND	GND	GND		
GND				•	

					TX to RX and RX to RX				GNE	GND				
			GND	GND			GND	GND	GND	RXP3 207	RXN3 207	GND	GND	PCB GND VIA
GND	GND	GND	TXP3 207	TXN3 207	GND	GND	GND	RXP2 207	RXN2 207	GND	GND	RXP1 207	RXN1 207	PCB GND VIA
GND	TXP2 207	TXN2 207	GND	GND	TXP1 207	TXN1— 207	GND	GND	GND	RXP0 207	RXN0 207	GND	GND	PCB GND VIA
GND	GND	GND	TXP0 207	TXN0 207	GND	GND	GND	RXP3 206	RXN3 206	GND	GND	RXP2 206	RXN2 206	PCB GND VIA
GND	TXP3 206	TXN3 206	GND	GND	TXP2 206	TXN2 206	GND	GND	GND	RXP1 206	RXN1 206	GND	GND	PCB GND VIA
GND	GND	GND	TXP1 206	TXN1 206	GND	GND	GND			GND	GND			
			GND	GND				-				•		V00007 05110

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GTM transceivers can operate at data rates up to 112 Gbps by using two out of the four transceivers in each Quad. As illustrated in the following figure, by choosing one of (Lane0 or Lane1) and one of (Lane2 or Lane3) in a Quad, both TX-to-TX and RX-to-RX crosstalk are limited to one diagonal aggressor. Therefore, the minimum isolation targets are easier to achieve without strict layout guidelines.

		GND	GND	RX to	RX			TX to	o TX	GND	GND			GND
GND	GND	RXP3 207	RXN3 207	GND	GND	PCB GND VIA	GND	GND	GND	TXP3 207	TXN3 207	GND	GND	GND
RXP2 207	RXN2 207	GND	GND	RXP1 207	RXN1 207	PCB GND VIA	GND	TXP2 207	2 TXN2 207	GND	GND	TXP1 207	TXN1 207	GND
GND	GND	RXP0 207	RXN0 207	GND	GND	PCB GND VIA	GND	GND	GND	TXP0 207	TXN0 207	GND	GND	GND
RXP3 206	RXN3 206	GND	GND	RXP2 206	RXN2 206	PCB GND VIA	GND	TXP3 206	3 TXN3 206	GND	GND	TXP2 206	TXN2 206	GND
GND	GND	RXP1 206	RXN1 206	GND	GND	PCB GND VIA	GND	GND	GND	TXP1 206	TXN1 206	GND	GND	GND
		GND	GND					_		GND	GND		•	
				GND	, тх	to RX	GND	GND	GND			_		
				TXN	3 GNE	GND) GND	RXP2	2 RXN2					
				GNE	, TXP	1 TXN	1 GND	GND	GND					
				TXN	0 GNE	D GND) GND	RXP3	RXN3					
				GNE	TXP	2 TXN	2 GND	GND	GND					
				TXN	206 1 GNI	206 206								
				206 GNE										
				GINL	,		TX to PX	and PX to		GND	GND			
											RXN3			PCB
			GND	GND	-		GND	GND	GND	207	207	GND	GND (GND VIA
GND	GND	GND	1XP3 207	1XN3 207	GND	GND	GND	RXP2 207	RXN2 207	GND	GND	207	207 (PCB GND VIA
GND	TXP2 207	TXN2 207	GND	GND	TXP1 207	TXN1	GND	GND	GND	RXP0 I 207	RXN0 207	GND	GND	PCB GND VIA
GND	GND	GND	TXP0 207	TXN0 207	GND	GND	GND	RXP3 206	RXN3 206	GND	GND	RXP2 206	RXN2 206 (PCB GND VIA
GND	TXP3 206	TXN3 206	GND	GND	TXP2 206	TXN2 206	GND	GND	GND	RXP1 I 206	RXN1 206	GND	GND	PCB GND VIA
GND	GND	GND	TXP1 206	TXN1 206	GND	GND	GND			GND	GND			
			GND	GND										X28095-051123

Figure 12: BGA Pin Pattern Examples – 112 Gbps Dual

The crosstalk components depicted in Figure 6: Crosstalk Components are listed below and illustrated in the following figure.

- TX-to-TX coupling: Dominated by via-via coupling and occurs at BGA pin
- RX-to-RX coupling: Dominated by via-via coupling and occurs at BGA pin

Send Feedback



• TX-to-RX coupling: Dominated by trace-via coupling and occurs at RX BGA pin

Figure 13: Crosstalk Components in BGA Pin Field



PCB Stackup and Via Construction for Example PCB Breakout Design

An example PCB breakout design based on the C4072 package is provided to demonstrate good practices regarding BGA breakout optimization for crosstalk mitigation.

The PCB stackup and via construction used for the analysis are summarized as follows:

- 28-layer stackup with a total thickness of 131.9 mil
- Eight inner signal layers L3, L5, L7, L9, L20, L22, L24, and L26
- Via-in-pad
- EM890K PCB material (1035 × 1035) with HVLP copper foil for signal layers



Figure 14: 28-Layer Reference Stackup

Name FIMA total Thians Filad total Filad total Filad total Constrain Top SUDERMAX, IP, GREEN UNNAMED, DOI 0.8 delects: 0.8 delects: SUDERMAX, IP, GREEN UNNAMED, DOI 0.8 3.23 0.3 3.23 0.00 1.2, SND, SND, SND, SND, SND, SND, SND, SND				Layer	T hick ness	
Nate FibMa Stall Onto OR Object SUDERMAK, PL, GREEN UNNAMED DD1 TOP TOP FIL 2.3 conductor SUDERMAK, PL, GREEN UNNAMED DD1 TOP TOP FIL 2.3 conductor SUDERMAK, PL, CUD, SI2PS UNNAMED DD3 L3, 400, FIL 0.6 5.31 conductor SUDERMAK, PL, CUD, SI2PS L3, 400, FIL 0.6 5.31 conductor 6.31 conductor SUDERMAK, PL, CUD, SI2PS L3, MGTD1 L3, MGTD1, FIL 0.6 3.31 conductor 3.31 conductor SUDERMAK, PL, CUD, SI2PS L3, MGTD2 L3, MGTD2, FIL 0.6 3.31 conductor 3.32 conductor 3.32 conductor 3.32 conductor 3.32 conductor 3.32 conductor </th <th></th> <th></th> <th></th> <th>Thickness</th> <th>from Top</th> <th></th>				Thickness	from Top	
DIDERMAK, IP, GREEN UNVAMED D01 D02 D02 delects D01 EMBOR 1 XID78 RGB PRG IPALD R2794 UNVAMED D03 IA1 2.3 2.3 2.3 Double State 2.3 2.3 Double State 2.3 2.3 Double State 2.3 D.3 Double State DOUBLE State D.3 Double State Double Stat	Material	Name	FilMaterial	(mis)	(mils)	Туре
1402_RATE 2*5 107 TOP TOP FIL 2.3] onductr 1010_EMBORS 12007 R40 P R50 FML 0x2PM WANAMED 003 1.41 5.81 dedicting 002_FMR_CU_DK3P26 12_0 ND 12_0 ND 12_0 ND 10.01 <td< td=""><td>SOLDERMASK LPI GREEN</td><td>UNNAMED 001</td><td></td><td>0.8</td><td></td><td>delectric</td></td<>	SOLDERMASK LPI GREEN	UNNAMED 001		0.8		delectric
Dit LEMBOR Läutor # 600 PR 65 JPR 10 DK2PH LVN AMED 003 1.4.1 5.8.1 Selectric Dit LEMBOR LÄUDER #004 CORE JPD DK2PH LVN MOT LE GND, FILL 0.6 6.5.1 Dit Mondutor Dit MARKEL LÄUDER #004 CORE JPD DK2PH LVM GF01 LE MARCI JUNER #004 0.6 11.1 Dit Mondutor Dit MARKEL LÄUDER #004 PRG JP735 DK2PH LVM GF01 LE MARCI JUNER #004 PRG JP735 DK2PH LVM AMED 008 1.4 Dit Mondutor DID MARKEL LÄUDER #004 PRG JP735 DK2PH LVM AMED 014 J4.4 DIT MONDUTOR DIT MONDUTOR DIT MONDUTOR DIT MONDUTOR J4.5 DIT MONDUTOR DIT MONDUTOR<	A30Z PLATED 2P5	TOP	TOP FILL	2.5	2.5	conductor
070.2, FMP, 2 (U) RX 325 12, 6 ND 12, 6 ND, 7 LL 0.6 6, 51, 6 noductor 070.2, FMP, 2 (U) RX 325 13, M GT01, 7 LL 0.6 13, 11, 6 noductor 070.2, FMP, 2 (U) RX 325 13, M GT01, 7 LL 0.6 14, 7 14, 58, 6 delectric 070.2, FMP, 2 (U) RX 325 12, M GT01, 7 LL 0.6 14, 6 delectric 14, 8 delectric 070.2, FMP, 2 (U) RX 125 13, 18, 6 noductor 14, 6 MO 14, 6 MO 14, 6 MO 14, 8 Mortor, 7 MU 0.6 13, 18, 6 noductor 070.2, FMP, 2 (U) RX 125 12, 15, M GT02 15, M GT02, FUL 0.6 14, 6 MO 14, 7 MU 0.6, 12, 2, 8 G, 6 noductor 14, 7 MU 14, 7 M A A A A A A A A A A A A A A A A A A	001-EM890K-1X1078-RC69-PREG-3P41-0K2P94	UNNAMED 003	-	3.41	5.91	dielectric
Dial Marken Datas Rock COR 1200 DATA UNAMED DBS Marcine 4 10.51 deleters 032 (MAPS CU DATAS [L] MATOL [L] MATOL 10.4 0.6 11.11 conductor 033 (MAPS LIXIDS RCAP REG 1973 5 DK2PH UNAMED 008 [L] MATOL 0.6 15.11 conductor 033 (MAPS LIXIDS RCAP REG 1973 5 DK2PH UNAMED 011 0.6 15.13 conductor 033 (MAPS LIXIDS RCAP REG 1973 5 DK2PH UNAMED 014 0.7 1.47 21.25 delects 030 (MAP CU DK2PS [L] MATOL 0.6 1.5.13 conductor 0.6 21.85 conductor 030 (MAP CU DK2PS [L] MATOL 1.6 GNO RL 0.6 2.8.25 conductor 030 (MAP CU DK2PS [L] MATOL 1.6 GNO RL 0.6 2.8.25 conductor 030 (MAP CU DK2PS [L] MATOL [L] MATOL 0.4 4.7 2.1.25 delects 030 (MAP CU DK2PS [L] MATOL [L] MATOL 0.6 3.2.2 conductor 0.0 031 (MAP CU DK2PS [L] MATOL 1.1 0.0 1.1 1.1 1.1 1.1 1.1 1.1	05DZ HVLP CU DK3P26	LZ GND	LZ GND FILL	0.6	6.51	conductor
002, HM2, CU DK 1975 [L], MGT01. [L], MGT01. B.4 0.6 11.11 conductor 033, MM50K, LXIDS RCOP PEGE 1973 50 K2PM [L], GGND L4, GND, RLL 0.6 15.18 conductor 030, MM50K, LXIDS RCOP PEGE 1973 50 K2PM LM, GND, RLL 0.6 15.18 conductor 1.11 conductor 031, MM50K, LXIDS RCOP PEGE 1973 50 K2PM LM, MAND 014 2.47 2.12 conductor 032, MM2, CU DK 2PS LG, GND LG, GND, RLL 0.6 2.12 conductor 031, MM50K, LXIDS RCOP PEGE 1973 50 K2PM UNNAMED 014 4 2.73 conductor 032, MM2, CU DK 2PS LG, MNG XU DK 2PS LG, MNG XU DK 2PS LG, GND RLL 0.6 52.25 conductor 032, MM5 CU DK 2PS LG, NNAMED 020	002 EM890K-1X1035 R066 CORE-2P0-0K2P98	UNNAMED 005		4	10.51	dielectric
Dia E MARRO I, XILOS R.GO. PREG. 1973.5 0.2194 UNAMED. 008 1.4 9.47 14.5 st delectric COOL MAP, C.U. DEP26 L/A GAD L/A GAD Statistic constructor SIG MARRO E, LINER REC. CORE. 200 DE2786 L/A GAD L/A GAD Statistic constructor GOD E, MAP, CU.D.K 226 LOD KEP26 L/S MARRO E, LINER REC. CORE. 200 DE2786 L/A GAD L/A Z.Z.Z. delectric GOD E, MAP, CU.D.K 2756 L/S GAD L/S GAD L/A Z.Z.Z. delectric GOD E, MAP, CU.D.K 2756 L/J MARRO DI L/A Z.Z.Z. delectric GAD L/S GAD L/S GAD L/A Z.Z.Z. delectric GAD	050Z HVLP CU DK3P26	L3 M GT01	L3 MGT01 FILL	0.6	11.11	conductor
DOZ, HAP, CU, DK 1976 [4, GND [4, GND </td <td>003 EM890K 1X1035 RC69 PREG 1P735 DK2P94</td> <td>UNNAMED 008</td> <td></td> <td>3.47</td> <td>14.58</td> <td>dielectric</td>	003 EM890K 1X1035 RC69 PREG 1P735 DK2P94	UNNAMED 008		3.47	14.58	dielectric
Dot Exercise Cale ALMOD 011 Cale ALMOD 011 <thcale 011<="" almod="" th=""> <thcale almod<="" td=""><td>05DZ HVLP CU DK3P26</td><td>L4 GND</td><td>L4 GND FILL</td><td>0.6</td><td>15.18</td><td>conductor</td></thcale></thcale>	05DZ HVLP CU DK3P26	L4 GND	L4 GND FILL	0.6	15.18	conductor
DOD. H.V.P. (U. D.K.PZ6 IS. MGT02 IS. MGT02 D.S. MGT02, FLL 0.6 19.75 conductor DOJ. EMARGIC LINIDS FGGD PREG 1973 5 D/2PM UNNAMED 014 0.6 23.25 dielectric DOJ. EMARGIC LINIDS FGGD PREG 1973 5 D/2PM UNNAMED 017 4 27.85 dielectric DOJ. EMARGIC LINIDS FGGD PREG 1973 5 D/2PM UNAMED 020 3.47 31.92 dielectric DOJ. EMARGIC LINIDS FGGD PREG 1973 5 D/2PM UNNAMED 020 3.47 31.92 dielectric DOJ. EMARGIC LINIDS FGGD PREG 1973 5 D/2PM UNNAMED 020 3.47 40.59 dielectric DOJ. EMARGIC LINIDS FGGD PREG 1973 5 D/2PM UNNAMED 026 3.47 40.59 dielectric DOJ. EMARGIC LINIDS FGGD PREG 1973 5 D/2PM UNNAMED 026 3.47 40.59 dielectric DOJ. EMARGIC LINIDS FGGD PREG 1973 5 D/2PM UNNAMED 027 6 45.79 dielectric DOJ. EMARGIC LINIDS FGG CORE 270 D/2PM UNNAMED 021 11.027 PMR FILL 0.6 46.39 dielectric DOJ. EMARGIC LINIDS FGG FREG 1973 5 D/2PM UNNAMED 031 11.202 FWR FILL 2.4 45.8 dielectric DOJ. EMARGIC LINIDS FGG FREG 1973 5 D/2PM UNNAMED 031 12.702 GND RLL 2.4	002 EM890K 1X1035 R056 CORE 2P0 DK2P98	UNNAMED 011		4	19.18	dielectric
Diss Disso R. 12003 F. 6020 PREG. 1973 5 D12P44 UWNAMED 0.14 Disso R. 11 Disso R 11 Disso R. 11 <t< td=""><td>050Z HVLP CU DK3P26</td><td>L5 M GT02</td><td>L5 MGT02 FILL</td><td>0.6</td><td>19.78</td><td>conductor</td></t<>	050Z HVLP CU DK3P26	L5 M GT02	L5 MGT02 FILL	0.6	19.78	conductor
DOZ 1. MUP CU DK 1975 L6 GND L6 GND L6 GND R11 O.6 23 28 Strong LATCOS RCGS CORE 200 DK298 LVMAMED D17 6 23 a Strong LATCOS RCGS LY73 50 DK2994 LVMAMED D20 17 MGTO3 L1 MGTO3	003 EM890K 1X1035 RC69 PREG 1P735 DK2P94	UNNAMED 014		3.47	23.25	dielectric
NO. EXAMPLE 11/015 RGG PREG 1073 DK2PM LVM AMED 017 AGE Additation 0502 HVLP, CU DK3P25 LV MAMED 020 1.47 31.92 delectric 0502 HVLP, CU DK3P25 LV MAMED 020 1.47 31.92 delectric 0502 HVLP, CU DK3P25 LV MAMED 020 4.47 31.92 delectric 0502 HVLP, CU DK3P25 LV MAMED 021 4 36.92 delectric 0502 HVLP, CU DK3P35 LV MAMED 025 3.47 40.59 delectric 0502 HVLP, CU DK3P33 LUD 1002 GMD LD 102 GMD RLL 1.2 41.79 conductor 0503 EM80K LX1003 RGG PREG 10735 DK2PM LVM AMED 031 4.5.7 45.57 delectric 4.5.7 0502 HVLP, CU DK3P35 LUD 102 GMD L12 102 GMD RLL 2.4 4.5.8 delectric 003 EM80K LX1003 RGG PREG 10735 DK2PM LVM AMED 031 1.4.7 4.5.7 delectric 4.5.7 delectric 003 EM80K LX1003 RGG PREG 10735 DK2PM LVM AMED 034 1.2 2.5 5.4.76 delectric 5.2.5 delectric 5.2.5 delectric 5.2.5 delectric 5.2.5 delectric 5.2.5 dele	050Z HVLP CU DK3P26	L6 GND	LS GND FILL	0.6	23.85	conductor
SGOZ WVLP CU DK3725 L7 MGT03 L7 MGT03 PILL 0.6 28.45 conductor SGOZ WVLP CU DK3725 LG GND LE GND PILL 0.6 31.92 delectric SGOZ WVLP CU DK3725 LG GND LE GND PILL 0.6 31.92 delectric SGOZ WVLP CU DK3725 LG GND LE GND PILL 0.6 31.92 delectric SGOZ WVLP CU DK3725 LG MGT04 LG MGT04 PILL 0.6 31.92 delectric SGOZ WVLP CU DK3725 LG MGT04 LG MGT04 PILL 0.6 31.71 20 onductor SGOZ WVLP CU DK3725 LG MGT04 LG NGT04 PILL 0.6 45.79 delectric SGOZ WVLP CU DK3733 LG 102 CWP CU DK3725 LG 102 CWP CU 0.44 45.79 delectric SGOZ WVLP CU DK3733 LG 102 CWP CU DK3733 LG 20 CWP CU 3.47 40.56 delectric SGOZ WVLP CU DK3733 LG 102 CWP CU DK3733 LG 20 CWP CU 3.47 40.56 delectric SGOZ WVLP CU DK3733 LG 20 CWP NR LG 20 CWP NR LG 20 CWP NR 2.44 5.22 Genductor SGOZ WVLP CU DK3733 LG 20 CWP NR LG 20 CW	002 EM890K-1X1035 R066 CORE-2P0 DK2P98	UNNAMED 017		4	27.85	dielectric
D33 EMBSOL 1X1005 RG05 PREG 19735 D K2P94 LNN AMED 020 18 GND RLL 0.6 32.52 conductor 0502 FWLP, CU D K3P25 LS GND CHI 18 GND RLL 0.6 32.52 conductor 0502 FWLP, CU D K3P25 LS MATOL 12 48 E12 dedectic 48 E12 dedectic 0502 FWLP, CU D K3P33 LD 102 GND RLL 0.6 37.12 conductor 0502 FWLP, CU D K3P33 LD 102 GND RLL 1.2 41.79 conductor 0502 FWLP, CU D K3P33 LD 102 GND RLL 1.2 41.79 conductor 0502 FWLP, CU D K3P33 LD 102 GND RLL 2.4 45.79 dedectric 0502 FWLP, CU D K3P33 LD 102 GND RLL 2.4 45.79 dedectric 0502 FWLP, CU D K3P33 LD 102 GND RLL 2.4 52.56 conductor 0502 FWLP, CU D K3P33 LD 102 GND RLL 2.4 52.56 conductor 0502 FWLP, CU D K3P33 LD 102 GND RLL 2.4 57.15 conductor 0503 FWLP, CU D K3P33 LD 102 GND RLL 2.4 57.15 conductor 0504 FWLP, CU D K3P33 LD 202 FWR LL1 202 FWR FILL 2.4 57.16 conductor 050 FWLP CU D K3P33 LD 20	050Z HVLP CU DK3P26	L7 M GT03	L7 MGT03 FILL	0.6	28.45	conductor
CSOZ IVAP CUID DK3P26 LB END LB GND RLL 0.6 32.52 conductor D32 EMBORIN LINDIS RC66 CORE 1PD DK2PSE LISM GTOL LIS MGTOL RLL 0.6 37.12 conductor 003 EMBORIN LINDIS RC69 PREG 1P735 DK2P54 LISM GTOL LIS MGTOL 1.12 CAT.PD DK2P33 LID<102 GND	003 EM890K-1X1035 RC69 PREG 1P735 D K2P94	UNNAMED 020		3.47	31.92	dielectric
D22 EMERON 3 JUDIS RGS-CORE 1PD DK/IPSE DNNAMED 023 4 36.52 delectric 030.2, MLVP CU_DK3P33 US_MOTAL US_MOTAL 0.6 37.12 conductor 030.3, MKSOK LINDES RGS-PRES 1P735 DK2P34 UNNAMED 026 37.47 0.53 delectric 020.2, MKSOK LINDES RGS-CORE 2PD DK2P35 UNNAMED 025 445.79 delectric 030.2, MKSOK LINDES RGS-CORE 2PD DK2P35 UNNAMED 021 3.47 45.86 delectric 030.2, VLP, CU_DK3P33 UL1 202, FWR 111 202 FWR FILL 0.6 46.39 conductor 030.3, VLP, CU_DK3P33 UL1 202, FWR 112 102 GAND RILL 2.4 57.26 conductor 030.2, VLP, CU_DK3P33 UL12 102 GAND 112 202 FWR 113 202 FWR 12.4 57.56 conductor 020.2, VLP, CU_DK3P33 UL12 202 FWR 113 202 FWR 114 202 FWR 2.4 57.56 conductor 021.6, VLP, CU_DK3P33 UL3 202 FWR FILL 2.4 57.56 conductor 021.6, VLP, CU_DK3P33 UL3 202 FWR FILL 2.4 57.52 conductor 021.6, VLP, CU_DK3P33 UL12 202 FWR FILL 2.4 57.84 delectric	050Z HVLP CU DK3P26	L8 GND	LS GND FILL	0.6	32.52	conductor
DSGZ HALP CU DK3P26 US MGT04 L9 MGT04 RILL 0.6 37.12 conductor D03 EM8SOK L1005 RC60 PREG 1P73 5 DK1P94 UNNAMED 026 3.47 40.59 delectric D02 EM8SOK L1005 RC62 CORE 2/D DK1P98 UNNAMED 029 4 45.79 delectric D02 EM8SOK L1005 RC62 CORE 2/D DK1P98 UNNAMED 029 4 45.79 delectric D03 EM8SOK L1005 RC62 CORE 2/D DK1P98 UNNAMED 031 3.47 49.86 delectric D03 EM8SOK L1005 RC62 CORE 2/D DK1P98 UNNAMED 031 3.47 49.86 delectric D02 EM1702 L1007 RC58 CORE 2/D DK1P94 UNNAMED 034 2.5 53.76 delectric D02 EM1702 L1007 RC58 CORE 2/D DK1P94 UNNAMED 036 4.28 51.45 delectric D02 VP CU DK3P33 L13 202 PWR L13 202 PWR 4.24 53.47 delectric D02 VP CU DK3P33 L14 202 PWR CENTER FILL 2.4 63.84 delectric 2.02 D01 EM1702 L1006 RC75 PREG 2P03 DK2P94 UNNAMED 041 2.4 63.84 delectric 2.02 D02 VP CU DK3P33 L15 202 PWR CENTER FILL 2.4 63.84 delectric 2.02 D02 VP CU DK3P33 L15 202 PWR CENTER FILL	002 EM890K-1X1035-R066-C0RE-2P0-0K2P98	UNNAMED 023		4	36.52	dielectric
033 EMSSOIL 1X1033 RCE0P PREG 1P735 D X2P94 UNNAMED 026 3.47 40.59 delectric 102 VUP_CU_CKXP73 UD_102_G ND LLD_102_G ND_RLL 1.2 41.78 donaductor 0030 EMSSOIL X1033 RCSC COME 2P D CK2P93 UNNAMED 029 4 44.77 delectric 0030 EMSSOIL X1033 RCSC COME 2P D CK2P93 UNNAMED 031 3.47 44.83 donaductor 0032 EMSSOIL X1033 RCSB PREG 1P735 D X2P94 UNNAMED 031 3.47 44.85 delectric 0032 EMSSOIL X1035 RCSB PREG 1P735 D X2P94 UNNAMED 031 3.47 44.85 delectric 003 EMSTOIL X1055 RCSB PREG 2P73 D X2P94 UNNAMED 034 2.4 51.7.16 conductor 004 EMSTOIL X1056 RCTS PREG 2P73 D X2P94 UNNAMED 039 42.8 61.44 delectric 020 VUP_CU_D CK2P33 LLS_202_FWR LLS_202_FWR_CENTER 12.4 66.84 delectric 020 VUP_CU_D CK2P33 LLS_202_FWR LLS_202_FWR_FILL	050Z HVLP CU DK3P26	L9 M GT04	L9 MGT04 FILL	0.6	37,12	conductor
102 VLP_CU_DK3P33 L10_102_GND L10_102_GND_RLL 1.2 41.79 conductor 002 VLP_CU_DK3P33 UNAAMED_029 4 45.79 deleteric 003 VLP_CU_DK3P33 UNAAMED_031 347 45.86 deleteric 003 VLP_CU_DK3P33 UL1_207_FWR L11_207_GND_RLL 24 52.26 conductor 102 VLP_CU_DK3P33 UL2_107_GND L12_107_GND_RLL 24 52.26 conductor 102 VLP_CU_DK3P33 UL3_207_FWR L13_207_FWR L12_24 57.16 conductor 202 VLP_CU_DK3P33 UL3_207_FWR L13_207_FWR L14_24 57.16 conductor 202 VLP_CU_DK3P33 UNAAMED_036 -42.8 61.44 deleteric 202 VLP_CU_DK3P33 UNAAMED_041 24.8 63.84 deleteric 202 VLP_CU_DK3P33 UNAAMED_041 24.8 73.52 deleteric 202 VLP_CU_DK3P33 UNAAMED_041 24.8 73.52 deleteric 202 VLP_CU_DK3P33 UNAAMED_041 25 78.42 deleteric 202	003 EM890K-1X1035 R069 PREG-1P735 DK2P94	UNNAMED 026		3.47	40.59	delectric
D22 EMERION LILID3R ACIA GORE 2PD DK2P98 UNNAMED 029 4 417.79 deleterin 0502 FWLP CU_DK3P36 L11_202_PWR L11_202_PWR FILL 0.5 46.39 conductor 033 EMESION LILID3R ACIA PREG_IP735 DK2P94 UNNAMED 031 347 44.85 deleterin 102 VLP_CU_DK3P33 L12_10Z_GND L12_10Z_GND_RLL 2.4 55.25 conductor 029 EMEMON LILO7R ACI38 CORE 2P5 DK3P16 UNNAMED 034 2.3 54.76 deleterin 020 VLP_CU_DK3P33 L13_20Z_PWR L13_20Z_PWR_FILL 2.4 55.16 conductor 020 VLP_CU_DK3P33 L13_20Z_PWR EL14_20Z_PWR_CENTER_FILL 2.4 63.84 deleterin 020 VLP_CU_DK3P33 L13_20Z_PWR_CENTER_LILS_20Z_PWR_CENTER_FILL 2.4 63.84 deleterin 020 VLP_CU_DK3P33 L15_20Z_PWR_CENTER_FILL 2.4 63.84 deleterin 020 VLP_CU_DK3P33 L15_20Z_PWR_CENTER_FILL 2.4 63.84 deleterin 020 VLP_CU_DK3P33 L16_20Z_PWR L15_20Z_PWR_FILL 2.4 75.92 conductor 020 VLP_CU_DK3P33 L16_20Z_PWR L15_20Z_PWR_FILL 2.4 75.92 conductor 020 VLP_CU_DK3P33 L13_10	10Z VLP CU DK3P33	L10 10Z GND	LID 10Z GND FILL	1.2	41.79	conductor
DSDZ_HVLP_CU_DK3P26 L11_202_PWR L11_202_PWR_FILL 0.6 46.39 conductor D03_EN4890K_1X1035_RC69_PREG_IP735_DK2P4 LVMAAMED_031 3.47 49.86 delectric D03_EN4890K_1X1035_RC69_PREG_IP735_DK2P4 LVDAMAMED_031 2.4 52.26 conductor D04_EN4702_1X1078_RC58_C0RE_2P5_DK2P4 LVDAMAMED_034 2.5 54.76 delectric D05_EN4702_1X1056_RC51_C0RE_3P5_DK2P4 LVMAAMED_036 4.22 61.44 delectric D05_EN4702_1X1056_RC51_C0RE_3PD_DK2P4 LVMAAMED_036 4.22 61.44 delectric D02_EV_P_CU_DK3P33 L14_202_PVWR_CENTER L12_202_PVWR_CENTER_FILL 2.4 63.48 donductor D02_EV_P_CU_DK3P33 L15_202_PWWR_CENTER L15_202_PWWR_CENTER_FILL 2.4 63.24 conductor D02_EV_P_CU_DK3P33 L15_202_PWWR_CENTER L15_202_PWWR_FILL 2.4 63.24 conductor D02_EV_P_CU_DK3P33 L15_202_PWWR_ENTER L15_202_PWWR_FILL 2.4 63.24 conductor D02_EV_P_CU_DK3P33 L15_202_PWWR_ENTER L15_202_PWR_FILL 2.4 68.08 conductor D02_EVATO2_X10050_RC175_PREG_2P03.DK2P4 LVNAAMED_044 2.5 28.58 delelectric	002 EM890K-1X1035-R066-C0RE-2P0-0K2P98	UNNAMED 029		4	45.79	dielectric
003 EM890K 1X1035 RCE9 PREG 1773 5 DK2P44 UNNAMED 031 3.47 49.86 delectric 102 VUP, CUD KKP33 L12 102 G ND L12 102 G ND FILL 2.4 52.26 conductor 202 VUP, CUD KKP33 L13 202 PWR L13 202 PWR L13 2.4 57.16 conductor 202 VUP, CUD KKP33 L13 2.02 PWR FILL 2.4 57.16 conductor 203 FLR3702 XL0060 RC75 PREG 2.00 XK1923 L14 2.02 PWR CHTER FILL 2.4 69.24 conductor 204 FLQ DK8733 L15 2.02 PWR ELTS 2.02 PWR ELTS 2.4 69.24 conductor 204 FLQ DK8733 L15 2.02 PWR L15 2.02 PWR FILL 2.4 69.24 conductor 202 VLP DL0 KR733 L17 1.02 G ND FILL 2.4 86	050Z HVLP CU DK3P26	L11 20Z-PWR	L11 202 PWB FILL	0.6	46.39	conductor
102 VLP_CU_DK3P33 L12_10Z_GND L12_10Z_GND_RLL 2.4 S2.26 conductor 009 EM3702_IX1078_RCS8_CORE_2PS_0K1P16 UNNAMED_014 25 S4.76 deloctric 000 EM3702_IX1078_RCS8_CORE_2PS_0K1P16 UNNAMED_036 4.28 61.14 deloctric 008 EM3702_IX1060_RC75_PRE_G_2P03_DK2P4 UNNAMED_036 4.28 61.44 deloctric 202_VLP_CU_DK3P33 L14_202_PWR_CENTER L14_202_PWR_CENTER_FILL 2.4 69.24 conductor 202_VLP_CU_DK3P33 L15_202_PWR_CENTER L14_202_PWR_CENTER_FILL 2.4 69.24 conductor 202_VLP_CU_DK3P33 L15_202_PWR_CENTER L15_202_PWR_CENTER L14_20 73.52 deloctric 202_VLP_CU_DK3P33 L15_202_PWR_CENTER L15_202_PWR_FILL 2.4 69.24 conductor 203_VLP_CU_DK3P33 L15_202_PWR_CENTER L12_102_GRD_R1L 1.2 73.52 deloctric 204_VLP_CU_DK3P33 L15_202_PWR_ENTER L14_202_CPWR_FILL 2.4 68.08 conductor 205_VLP_CU_DK3P33 L15_102_GRD_R1L 1.2 73.52 deloctric 10.2 205_VLP_CU_DK3P33 L12_102_GRD_R1L	003 EM890K-1X1035 R069 PREG-1P735 DK2P94	UNNAMED 031		3.47	49.86	delectric
DD END TO Data Structure Data Structure Data Structure D02 END TO DX12 DX2 PWR L13 202 PWR END TO	107 VIP CII DK3P33	L12 107 GND	112 107 GND BU	2.4	52.26	conductor
202 VLP_CU_DIG3P3.3 L13_202_PWR L13_202_PWR L13_202_PWR L14_202_PWR <	009-EM3707-1X1078-BC58-C08E-725-DK3216	LINNAMED 034		2.5	54.76	delectric
Disc Disc <thdisc< th=""> Disc Disc <thd< td=""><td>207 VIP CII DK3P33</td><td>113 207 PWR</td><td>113 207 PWB FILL</td><td>7.4</td><td>57.16</td><td>conductor</td></thd<></thdisc<>	207 VIP CII DK3P33	113 207 PWR	113 207 PWB FILL	7.4	57.16	conductor
Display and a construction Display and a construction Display and a construction D11 EM3702 XXX052 EM3702 XXX052 EM3702 XXX052 EM3702 XXX052 EM3702 XXX050 EM3702 XXX072 EM3702 XXX072 EM3702 XXX072 EM3702 XXX072 EM3702 XX072 X	008-EM3707-1X1060-BC75-PREG-7P03-DK7 P94	UNNAMED 036		4.78	61.44	delectric
Dil EM3702 IXI0366 RC61 CORE 3P0 DK3P16 UNNAMED 0.39 Dil EM3702 IXI0366 RC61 CORE 3P0 DK3P16 UNN AMED 0.019 Dil EM3702 IXI0366 RC75 PRE G 2003 DK2 P94 UNN AMED 0.41 4.28 73.52 delectric 202, VLP_CU_DK3P33 LI5_20Z_PWR_LENTER LI5_20Z_PWR_ENTER LI5_20Z_PWR_ENTER 1.24 75.92 conductor 202, VLP_CU_DK3P33 LI5_20Z_PWR_ENTER LI5_20Z_PWR_ENTER 1.24 75.92 conductor 102, VLP_CU_DK3P33 LI5_20Z_PWR_ENTER LI5_20Z_PWR_ENTER 1.24 75.92 conductor 102, VLP_CU_DK3P33 LI5_20Z_PWR_ENTER LI5_20Z_PWR_FILL 2.4 85.86 delectric 202, VLP_CU_DK3P33 LI5_20Z_PWR_ENTER LI5_20Z_PWR_FILL 2.4 86.08 conductor 203, VLP_CU_DK3P33 LI3_10Z_GND LI3_10Z_GND 1.12 28.88 delectric 204, VLP_CU_DK3P33 LI3_10Z_GND L13_10Z_GND 1.12 28.78 delectric 204, VLP_CU_DK3P33 LI3_10Z_GND L13_10Z_GND 1.21 28.78 delectric 205, VLP_CU_DK3P35 LI3_10Z_GND L13_10Z_GND 1.21 28.78 delectric 205, VLP_CU_DK3P25 L20_SIG L20_SIG_FILL	207 VIP CII DK3P33	114 207 PWR CENTER	114 207 PWR CENTER FUL	7.4	63.84	conductor
202 VLP_CU_DK3P33 L15_202_PWR_CENTER L15_202_PWR_CENTER_FILL 2.4 69.24 conductor 008 EM3702_IXL060_RC75_PREG_2P03_DK2_P94 UNNAMED_041 4.28 73.52 delectric 202_VLP_CU_DK3P33 L16_202_PWR_FILL 2.4 75.92 conductor 009 EM3702_IXL058_RC58_CORE_2P5 DK3P16 UNNAMED_044 2.5 78.42 delectric 102_VLP_CU_DK3P33 L17_102_GND L17_102_GND_RLL 1.2 79.62 conductor 108_EM3702_IXL078_RC58_CORE_2P5 DK3P16 UNNAMED_046 4.06 83.68 delectric 102_VLP_CU_DK3P33 L19_102_GND L19_102_GND_RLL 1.2 88.58 delectric 102_VLP_CU_DK3P33 L19_102_GND L19_102_GND_RLL 1.2 88.78 conductor 104_VLP_CU_DK3P33 L19_102_GND L19_102_GND_RLL 1.2 88.78 conductor 105_VLP_CU_DK3P33 L19_102_GND L19_102_GND_RLL 1.2 88.78 conductor 004_EM390K1X1035_RC69_PREG_1P69_DK2P94 UNNAMED_051 3.39 93.17 delectric	011-EM370Z-1X1086-RC61-CORE-3P0.0K3P16	UNNAMED 039		3	66.84	dielectric
008 EM3702 1X1060 RC 75 PREG 2P03 UNNAMED_041 4.28 73.52 delectric 202 VUP_CU_DKIP33 L16 202_FWR L16 202_FWR L12 24 75.92 conductor D9 EM3702 1X1078 RCS8 CORE 2P5 D K3P16 UNNAMED_044 2.5 78.42 delectric D09 EM3702 1X1060 RCTS PREG 2P03 L17 102 G ND L17 102 G ND L12 79.62 conductor D08 EM3702 1X1060 RCTS PREG 2P03 UNNAMED_046 4.06 83.68 delectric D07 UVP_CU_DK3P33 L19 102 G ND L19 102 G ND RIL 1.2 89.78 conductor D05 EM390K 1 X1035 RC69 REG IP69 D K2P44 UNNAMED_051 3.39 93.17 delectric D502_HVLP_CU_DK3P26 L21_GND L21_GND_FILL 0.6 98.37 conductor D03_EM390K 1 X1035 RC69	20Z VLP CU DK3P33	L15 20Z PWR CENTER	L15 20Z PWR CENTER FILL	2.4	69.24	conductor
Z02_VUP_CU_DK3P33 L16_202_PWR L16_202_PWR_FILL 2.4 75.92 conductor D09_EM3702_IXL003_RC58_CORE_2P5_DK3P16 UNNAMED_044 2.5 78.42 delectric D07_EM3702_IXL005_RC58_CORE_2P5_DK3P16 UNNAMED_046 L17_10Z_GND_RLL 1.2 79.62 conductor D08_EM3702_IXL005_RC75_PREG_IP03_DK2P94 UNNAMED_046 4.06 83.68 delectric 202_VUP_CU_DK3P33 L18_202_PWR L18_207_PWR_FILL 2.4 86.08 conductor D09_EM3702_IXL005_RC58_CORE_2P5_DK3P16 UNNAMED_049 2.5 88.58 delectric D07_VUP_CU_DK3P33 L19_102_GND L19_102_GND_RLL 1.2 89.78 conductor D05_EM380K_IXL003_RC59_PREG_IP695_DK2P94 UNNAMED_051 3.39 93.17 dolectric D05_EM380K_IXL003_RC56_CORE_1P0_0K2P98 UNNAMED_057 3.47 101.84 delectric D05_EM380K_IXL003_RC56_CORE_1P73_5_DK2P94 UNNAMED_057 3.47 101.84 delectric D05_EM380K_IXL003_RC56_CORE_1P73_5_DK2P94 UNNAMED_057 3.47 101.84 <tddelectric< td=""> D05_EM380K_</tddelectric<>	008-EM370Z-1X1060-RC75-PREG-2P03-DK2P94	UNNAMED 041		4.28	73.52	delectric
D09 EM3702 DX10/78 RCS8 CORR ZPS 78 42 delectric 102 VLP_CU_DX3P33 L17_102_GND L17_102_GND_RLL 1.2 79.62 conductor 008 EM3702 IXL0050 RC75 PREG 2P03_DX2P94 UNNAMED_046 4.06 83.68 delectric 202 VUP_CU_DX3P33 L18 202_PWR L18_202_PWR L18_202_GND_RLL 2.4 86.08 conductor 009 EM3702 IXL078 RCS8 CORE_1P50 K294 UNNAMED_049 2.5 88.58 delectric 102 VUP_CU_DX3P33 L19_102_GND L19_102_GND_RLL 1.2 89.78 conductor 006 EM390X I XL038 RC69 PREG L20_SIG L20_SIG_FILL 0.6 93.77 conductor 0502_HVLP_CU_DK3P26 L21_GND L21_GND_FILL 0.6 98.37 conductor 0502_HVLP_CU_DK3P26 L22_SIG L22_SIG_FILL 0.6 102.44 conductor 0502_HVLP_CU_DK	20Z VLP CU DK3P33	L16 20Z PWR	L16 2OZ PWB FILL	2.4	75.92	conductor
102 VLP CU DK3P33 L17 102 GND L17 102 GND RLL 1.2 79.62 conductor 108 EM3702 IX1060 RC75 PRE G. 2P03 DK2 P94 UNNAMED_046 4.05 83.68 delectric 202 VLP CU DK3P33 L18 202 PWR FILL 2.4 86.08 conductor 109 EM3702 IX1078 RC58 CORE 2P5 88.58 delectric 107 VLP CU DK3P33 L19 102 GND L19 102 GND RLL 1.2 89.78 conductor 106 EM390K 1X1035 RC59 PREG. 1P955 L20 SIG FILL 0.6 93.77 conductor 0502 HVLP CU RX3P25 L21 GND L21 GND <fill< td=""> 0.6 102.44 conductor 0502 HVLP CU RX3P25 L22 <</fill<>	009-EM370Z-1X1078-RC58-CORE-2P5-0K3P16	UNNAMED 044		2.5	78.42	dielectric
DOB EM3702 IXI060 RC75 PRE G 2P03 DK2 P94 UNNAMED 046 4.06 83.68 dielectric 202_VUP_CU_DK3P33 L18_20Z_PWR L18_20Z_PWR FILL 2.4 86.08 conductor 006 EM3702 IXI078 RC58 CORE 2P5 DK3P16 UVNAMED 049 2.5 88.58 dielectric 102_VUP_CU_DK3P33 L19_10Z_GND L19_10Z_GND RUL 1.2 88.78 conductor 005 EM3702 IXI035 RC69 PREG 1P695 DK2P94 UNNAMED 051 3.39 93.17 dielectric 3.39 93.17 dielectric 0502_HVLP_CU_DK3P26 L20_SIG L20_SIG_FILL 0.6 98.37 conductor 0.6 0502_HVLP_CU_DK3P26 L21_GND L21_GND_FILL 0.6 98.37 conductor 0502_HVLP_CU_DK3P26 L22_SIG L22_SIG_FILL 0.6 10.2.44 conductor 033_EM890K IXI035 RC69 PREG IP735 D K2P94 UNNAMED 057 3.47 10.8.4 dielectric 0502_HVLP_CU_DK3P26 L22_SIG L22_SIG_FILL 0.6 107.04 conductor 034_EM890K IXI035 RC69 PREG IP735 D K2P94 UNNAMED 063 3.47 110.51 dielectric 0502_HVLP_CU_DK3P26 L23_GND L23_SID_FILL 0.6	10Z VLP CU DK3P33	L17 107 GND	L17 10Z GND FILL	1.2	79.62	conductor
ZOZ VUP CU DK3P33 L18 ZOZ PWR L18 ZOZ PWR FILL Z.4 S6.08 conductor D9 EM3702 1X1078 RC58 CORE ZPS DKZP16 UNNAMED 049 Z.5 88.58 delectric L02 VUP CU DK3P33 L19 10Z GND L19 10Z GND RLL 1.2 89.78 conductor D06 EM390K 1X1035 RC69 PREG 1P695 DKZP94 UNNAMED 051 3.39 93.17 delectric D052 HUP CU DK3P26 L20 SIG L20 SIG FILL 0.6 93.77 conductor D02 EM390K 1X1035 RC66 CORE 2P0 DKZP98 UNNAMED 054 4 97.77 delectric D03 EM390K 1X1035 RC69 PREG 1P735 DKZP94 UNNAMED 057 3.47 10.84 delectric D03 Z HVLP CU DK3P26 L21 GND L21 GND FILL 0.6 102.44 conductor D03 EM390K 1X1035 RC69 PREG 1P735 DKZP94 UNNAMED 060 4 106.44 delectric D502 HVLP CU DK3P26 L22 SG L23 GND FILL 0.6 107.04 conductor D03 EM390K 1X1035 RC69 PREG 1P735 DKZP94 UNNAMED 063 3.47 110.51 delectric D502 HVLP CU DK3P26 L23 GND L23 GND FILL 0.6 111.11 conductor D502 HVLP CU DK3P26 L24 SG SG<	008-EM370Z-1X1060-RC75-PREG-2P03-DK2P94	UNNAMED 046		4.05	83.68	delectric
D09 EM370Z 1X1078 RCS8 CORE 2PS DK3P16 UNNAMED 049 2.5 88.58 delectric 10Z_VLP_CU_DK3P33 L19_10Z_GND L19_10Z_GND_RLL 1.2 89.78 conductor 005 EM390K 1X1035 RC69 PREG 1P695 D K2P94 UNNAMED_051 3.39 93.17 delectric 050Z_HVLP_CU_DK3P26 L20_SIG L20_SIG_FILL 0.6 93.77 conductor 050Z_HVLP_CU_DK3P26 L21_GND L21_GND_FILL 0.6 98.37 conductor 003 EM390K 1X1035 RC66 CORE 2P0 DK2P98 UNNAMED_057 3.47 101.84 delectric 050Z_HVLP_CU_DK3P26 L22_SIG L22_SIG_FILL 0.6 102.44 conductor 003 EM390K 1X1035 RC66 CORE 2P0 DK2P98 UNNAMED 060 4 106.44 delectric 050Z_HVLP_CU_DK3P26 L23_GND L23_GND_FILL 0.6 107.04 conductor 003 EM390K 1X1035 RC66 CORE 2P0 DK2P98 UNNAMED 060 4 106.44 delectric 050Z_HVLP_CU_DK3P26 L24_GG L24_SIG_FILL 0.6 111.11 conductor 003 EM390K 1X1035 RC66 CORE 2P0 DK2P98	20Z VLP CU DK3P33	L18 207 PWR	L18 20Z PWB FILL	2.4	86.08	conductor
10Z_VUP_CU_DK3P33 [19]10Z_GND [19]10Z_GND [19]10Z_GND [12]10Z_GND [12]10Z_GND [12]10Z_GND [12]10Z_GND [13]10Z_GND [12]10Z_GND	009-EM370Z-1X1078-RC58-CORE-2P5-0K3P16	UNNAMED 049		2.5	88.58	dielectric
ODG-EM/SQC 1/1035 RC69 PREG 1P695 D K2P94 UNNAMED 051 3.39 93.17 delectric 0502 HVLP_CU_DK3P26 L20_SG L20_SG L20_SG L20_SG 93.77 conductor 0502 HVLP_CU_DK3P26 L20_SG L20_SG L20_SG 93.77 conductor 0502 HVLP_CU_DK3P26 L21_GND L21_GND L21_GND 93.77 conductor 003 EM890K 1X1035 RC66 CORE 2P0 DK2P98 UNNAMED 054 4 97.77 delectric 0502 HVLP_CU_DK3P26 L21_GND L21_GND L21_GND 3.47 10.84 delectric 0502 HVLP_CU_DK3P26 L22_SG L22_SG L22_SG 102.44 conductor 003 EM890K 1X1035 RC66 CORE 2P0 DK2P98 UNNAMED 060 4 106.44 delectric 0502 HVLP_CU_DK3P26 L23_GND L23_GND_FILL 0.6 107.04 conductor 003 EM890K 1X1035 RC69 PREG 1P735 D K2P94 UNNAMED 063 3.47 10.51 delectric 0502 HVLP_CU_DK3P26 L24_SG L24_SIG_FILL 0.6 111.11 conductor 03 EM890K	10Z VLP CU DK3P33	L19 107 GND	L19 10Z GND FILL	1.2	89.78	conductor
0502 HVLP_CU_DK3P26 L20_SIG L20_SIG_FILL 0.6 93.77 conductor 0502 HVLP_CU_DK3P26 L21_GND L21_GND_FILL 0.6 93.77 conductor 0502 HVLP_CU_DK3P26 L21_GND L21_GND_FILL 0.6 93.77 conductor 003 EM890K 1X1035 RC69 PREG 1P735 D K2P94 UNNAMED_057 3.47 10.84 delectric 0502 HVLP_CU_DK3P26 L22_SIG L22_SIG_FILL 0.6 100.244 conductor 003 EM890K 1X1035 RC66 CORE 2P0 DK2P98 UNNAMED_060 4 106.44 delectric 0502 HVLP_CU_DK3P26 L23_GND L23_GND_FILL 0.6 107.04 conductor 038 EM890K 1X1035 RC69 PREG 1P735 D K2P94 UNNAMED_063 3.47 110.51 delectric 0502 HVLP_CU_DK3P26 L24_SIG_FILL 0.6 111.11 conductor 052 HVLP_CU_DK3P26 L25_GND L25_GND_FILL 0.6 111.11 conductor <td< td=""><td>006-EM890K-1X1035-R069-PREG-1P695-DK2P94</td><td>UNNAMED 051</td><td></td><td>3 39</td><td>93.17</td><td>delectric</td></td<>	006-EM890K-1X1035-R069-PREG-1P695-DK2P94	UNNAMED 051		3 39	93.17	delectric
DOZ EM880K 1 X1035 RC66 CORE 2P0 DK2P98 UNNAMED 054 4 97.77 dielectric 0502 HVLP_CU_DK3P26 L21 GND L21 GND FILL 0.6 98.37 conductor 033 EM890K 1 X1035 RC69 PREG 1P73 5 D K2P94 UNNAMED 057 3.47 101.84 dielectric 0502 HVLP_CU_DK3P26 L22 SIG L22 SIG FILL 0.6 102.44 conductor 0502 HVLP_CU_DK3P26 L23 GND L23 GND FILL 0.6 102.44 conductor 0502 HVLP_CU_DK3P26 L23 GND L23 GND FILL 0.6 107.04 conductor 033 EM890K 1X1035 RC69 ORE 2P0 DK2P98 UNNAMED 060 4 105.1 dielectric 0502 HVLP_CU_DK3P26 L23 GND L24 SIG FILL 0.6 111.11 conductor 033 EM890K 1X1035 RC69 ORE 2P0 DK2P98 UNNAMED 063 3.47 110.51 dielectric 0502 HVLP_CU_DK3P26 L24 SIG L24 SIG FILL 0.6 111.11 conductor 034 EM890K 1X1035 RC69 OREG 1P735 D K2P94 UNNAMED 069 3.47 119.18 dielectric 0502 HVLP_CU_DK3P26 L25 GND L25 GND FILL 0.6 115.71 conductor 035 EM890K 1X1035 RC69 OREG 1P735 D K2P94 <td< td=""><td>050Z HVLP CU DK 3P26</td><td>L20 SIG</td><td>120 SIG FILL</td><td>0.6</td><td>93.77</td><td>conductor</td></td<>	050Z HVLP CU DK 3P26	L20 SIG	120 SIG FILL	0.6	93.77	conductor
050Z_HVLP_CU_DK3P26 L21_GND L21_GND_FILL 0.6 98.37 conductor 003_EM890K 1X1035_RC69_PREG_1P735_D K2P94 UNNAMED_057 3.47 101.84 delectric 050Z_HVLP_CU_DK3P26 L22_SIG L22_SIG_FILL 0.6 102.44 conductor 003_EM890K 1X1035_RC66_CORE_2P0_DK2P98 UNNAMED_060 4 106.44 delectric 050Z_HVLP_CU_DK3P26 L23_GND L23_GND_FILL 0.5 107.04 conductor 003_EM890K 1X1035_RC69_PREG_1P735_DK2P94 UNNAMED_063 3.47 110.51 delectric 050Z_HVLP_CU_DK3P26 L24_SIG L24_SIG_FILL 0.6 111.11 conductor 003_EM890K 1X1035_RC69_ORE_2P0_DK2P98 UNNAMED_066 4 115.11 delectric 050Z_HVLP_CU_DK3P26 L25_GND L25_GND_FILL 0.6 111.11 conductor 003_EM890K 1X1035_RC69_PREG_1P735_DK2P94 UNNAMED_069 3.47 119.18 delectric 050Z_HVLP_CU_DK3P26 L25_GND L25_SIG_FILL 0.6 119.78 conductor 050Z_HVLP_CU_DK3P26 L25_	002 EM890K-1X1035-R056-C0RE-2P0-0K2P98	UNNAMED 054		4	97.77	dielectric
OD3 EM890K 110035 RC69 PREG 1P73 5 D K2P94 UNNAMED 057 3.47 101.84 delectric 0502 FWLP_CU_DK3P26 L22_SIG L22_SIG_FILL 0.6 102.44 conductor 0502 FWLP_CU_DK3P26 L22_SIG L22_SIG_FILL 0.6 102.44 conductor 0502 FWLP_CU_DK3P26 L22_SIG L22_SIG_FILL 0.6 107.04 conductor 0502 FWLP_CU_DK3P26 L23_GND L23_GND_FILL 0.6 107.04 conductor 033 EM890K 1X1035 RC69 PREG 1P735 D K2P94 UNNAMED_063 3.47 10.51 delectric 0502 FWLP_CU_DK3P26 L24_SIG L24_SIG_FILL 0.6 111.11 conductor 032 EM890K 1X1035 RC66 CORE 2P0 DK2P98 UNNAMED_066 4 115.11 delectric 0502 FWLP_CU_DK3P26 L25_GND L25_GND_FILL 0.6 115.71 conductor 033 EM890K 1X1035 RC69 PREG 1P735 D K2P94 UNNAMED_069 3.47 119.18 delectric 0502 FWLP_CU_DK3P26 L25_SIG L25_SIG_FILL 0.6 115.71 conductor 0502 FWLP_CU_DK3P26	050Z HVLP CU DK3P26	L21 GND	121 GND FILL	0.6	98.37	conductor
Display Display Display Display Display Display	003 EM890K 1 X1035 B 059 PREG 1P73 5 D K2P94	UNNAMED 057		3.47	101.84	delectric
D02 EM880K 1 X1035 RC66 CORE ZPO DKXAMED 060 4 106.44 dielectric 0502 HVLP_CU_DK3P26 L23_GND L23_GND L23_GND_FILL 0.6 107.04 conductor 033 EM890K 1 X1035 RC69-PREG_1P735 D KZP94 UNNAMED_063 3.47 110.51 dielectric 0502_HVLP_CU_DK3P26 L24_SIG L24_SIG_FILL 0.6 111.11 conductor 0502_HVLP_CU_DK3P26 L24_SIG L24_SIG_FILL 0.6 111.11 conductor 0502_HVLP_CU_DK3P26 L25_GND L25_GND_FILL 0.6 115.71 conductor 0502_HVLP_CU_DK3P26 L25_GND L25_GND_FILL 0.6 115.71 conductor 033-EM890K 1X1035 RC69_PREG_1P735 D KZP94 UNNAMED_069 3.47 119.18 dielectric 0502_HVLP_CU_DK3P26 L26_SIG L26_SIG_FILL 0.6 119.78 conductor 022_EM890K 1X1035 RC66 CORE_2P0 DKZP98 UNNAMED_072 4 123.78 dielectric 0502_HVLP_CU_DK3P26 <td>050Z HVLP CU DK 3P26</td> <td>L22 SG</td> <td>122 SIG FILL</td> <td>0.6</td> <td>102.44</td> <td>conductor</td>	050Z HVLP CU DK 3P26	L22 SG	122 SIG FILL	0.6	102.44	conductor
0502_HULP_CU_DK3P26 L23_GND L23_GND_FILL 0.6 107.04 conductor 003_EM890K1X1035_RC69_PREG_1P735_D K2P94 UNNAMED_063 3.47 110.51 delectric 0502_HVLP_CU_DK3P26 L24_9G L24_9G L24_9G 111.11 conductor 0502_HVLP_CU_DK3P26 L24_9G L24_9G 125_GND_FILL 0.6 111.11 conductor 0502_HVLP_CU_DK3P26 L25_GND L25_GND_FILL 0.6 115.71 conductor 0502_HVLP_CU_DK3P26 L25_GND L25_GND_FILL 0.6 115.71 conductor 033_EM890K1X1035_RC69_PREG_1P735_DK2P94 UNNAMED_069 3.47 119.18 delectric 0502_HVLP_CU_DK3P26 L26_9G L26_9G_FILL 0.6 119.78 conductor 0502_HVLP_CU_DK3P26 L26_9G L26_9G_FILL 0.6 119.78 conductor 0502_HVLP_CU_DK3P26 L27_GND L27_GND_FILL 0.6 123.78 delectric 0502_HVLP_CU_DK3P26 L27_GND L27_GND_FILL 0.6 124.38 conductor 001_EM890K1X1078_RC69_PREG_3P41_0 K2P94 UNNAMED_075 3.41 127.79 delectric 430Z_PLATE_D_2P5	002-EM890K-121035-8056-C08E-2P0-0K2P98	LINNAMED 060		4	105.44	delectric
ODS_EMRSOK 11035 RC69 PREG 1P735 0 K2P94 UNNAMED_063 3.47 110.51 delectric 0502_EMRSOK 11035 RC69 PREG 1P735 0 K2P94 UNNAMED_063 3.47 110.51 delectric 0502_EMRSOK 11035 RC66 CORE_2P0_0K2P98 UNNAMED_066 4 115.11 delectric 0502_EMRSOK 11035 RC69 PREG 1P735 0 K2P94 UNNAMED_066 4 115.11 delectric 0502_EMRSOK 11035 RC69 PREG 1P735 0 K2P94 UNNAMED_069 125_GND_FILL 0.6 115.71 conductor 0502_EMRSOK 11035 RC69 PREG 1P735 0 K2P94 UNNAMED_069 3.47 19.18 delectric 0502_EMRSOK 11035 RC69 PREG 1P735 0 K2P94 UNNAMED_069 3.47 19.18 delectric 0502_EMRSOK 11035 RC69 PREG 1P735 0 K2P94 UNNAMED_072 4 123.78 delectric 0502_EMRSOK 11003 RC66 CORE 2P0 0 K2P98 UNNAMED_072 4 123.78 delectric 0502_EMRSOK 11078 RC69 PREG 3P41 0 K2P94 UNNAMED_075 3.41 127.79 delectric 0502_EMRSOK 112078 RC69 PREG 3P41 0 K2P94 UNNAMED_075 3.41 127.79 delectric 011_EMRSOK 112078 RC69 PREG 3P41 0	0507 HM P CIL DK 3P25	123 GND	123 GND FILL	0.5	107.04	conductor
0502 HVLP_CU_DK3P26 L24_SIG L24_SIG L24_SIG 111.11 conductor 0502 HVLP_CU_DK3P26 L24_SIG L24_SIG FILL 0.6 111.11 conductor 0502 HVLP_CU_DK3P26 L25_GND L25_GND_FILL 0.6 111.11 conductor 003 FMLSO HVLP_CU_DK3P26 L25_GND L25_GND_FILL 0.6 115.71 conductor 003 FMLSOK 110.35 RC69 PREG 1773.5 0K2P94 UNNAMED_069 3.47 119.18 delectric 0502 HVLP_CU_DK3P26 L25_SIG L26_SIG_FILL 0.6 119.78 conductor 0502 HVLP_CU_DK3P26 L26_SIG PIL 0.6 119.78 conductor 0502 HVLP_CU_DK3P26 L27_GND L27_GND_FILL 0.6 124.38 conductor 001 EMS90K 1X1078 RC69 PREG 3P41 0 K2P94 UNNAMED_075 3.41 127.79 delectric 430Z PLATE 0_2P5 B0TTOM SOLDERM	003 EM890K 1 X1035 B 059 PREG 1P73 5 D K2P94	UNNAMED 063		3.47	110 51	delectric
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SOLDERMASK_LPI_GREEN_1 UNNAMED_077 0.8 131.09 0.6 131.09 130.05 130.05 130.05 130.05 130.05 130.05 <th130.05< th=""></th130.05<>	4307 PLATED 2PS	BOTTOM	SOLDERMASK UPL OPEEN 1	3.41	120.79	conductor
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1 - Safe and - Safe an		and the other	Total PCB Thickness	131.89		



Figure 15: Via Construction



TX-to-TX/RX-to-RX Crosstalk Analysis for 56 Gbps Fulldensity Quad Usage

As shown in the following figure, the worst-case victim is in the middle column with four diagonal and two non-diagonal aggressors. The routing layers (via length) for the victim in the middle column and the two diagonal aggressors to the right of the victim are swept to visualize the effects of the via vertical parallelism to the crosstalk. The routing layer of the two diagonal aggressors to the left of the victim is kept to L24 (long vias) in the sweep analysis.



Figure 16: Victim with Four Diagonal and Two Non-Diagonal Aggressors

The following table lists the simulated power sum crosstalk for 56 Gbps PAM4 (at 14 GHz) for various routing cases. The data shows that the crosstalk amplitude correlates with the via vertical coupling length between victim and aggressors. A victim with four diagonal aggressors needs a via length < 45 mil to fulfill the -35 dB TX-to-TX power sum crosstalk requirement as stipulated in Table 1.





Powersum TX Xtalk (dB)	Victim Via Length (mil)	Aggressor Left Layer	Victim Center Layer	Aggressor Right Layer	Comments
-28.7 ¹	102.3	L24	L22	L22	Routed two layers (L22 and L24) long vias
-28.9 ¹	102.3	L24	L22	L20	Routed three layers (L20, L22, and L24) long vias
-34.6 ¹	44.1	L24	L11	L11	Routed two layers (L11 and L24) short vias
-34.0 ¹	54.6	L24	L13	L11	Routed three layers (L11, L13, and L24) short vias
-34.5 ¹	44.1	L24	L11	L22	Routed three layers (L11, L22, and L24) short vias
-35.9 ²	34.6	L24	L9	L22	Routed three layers (L9, L22, and L24) short vias
-37.8 ²	26	L24	L7	L22	Routed three layers (L7, L22, and L24) short vias
-38.7 ³	26	L24	L7	L7	Routed two layers (L7 and L24) short vias
-44.3 ³	8.6	L24	L3	L3	Routed two layers (L3 and L24) short vias
-40.3 ³	26	L24	L7	L3	Routed three layers (L3, L7, and L24) short vias

Table 2: Simulated TX-to-TX Power Sum Crosstalk per Via Length

Notes:

1. Not allowed.

2. OK with constraints.

3. Good.

4. This also applies to RX-RX.

TX-to-RX Crosstalk Analysis for 56 Gbps Full-density Quad Usage

Similarly, for the TX-to-RX crosstalk analysis of a triple-triple BGA pin pattern, the routing layers (via length) for the TX in the middle column are swept to understand the effects of vertical distance between TX lead-out traces and the RX via barrel to the TX-to-RX coupling.

- The routing layers for RX are constrained to L3, L5, and L7.
- The routing layer of the TX *middle* column is swept from L5, L7, L9, and L22.
- The routing layers of the TX right and left columns are kept to L22 and L24.

The following table lists the simulated power sum crosstalk for various cases. The following can be observed:

- The TX *middle* column is routed on a layer at least 18 mil (L9 L5) below the lowest RX routing layer to fulfill the -65 dB TX-to-RX crosstalk requirement.
- While routing the TX *middle* column on L22 minimizes TX-to-RX crosstalk, it violates the -35 dB TX-to-TX crosstalk requirement due to the long via vertical parallelism.
- The attainable RX-to-RX crosstalk is -44 dB, allowing a 14 dB victim-to-aggressor insertion loss delta.



PowerSum TX-TX Xtalk (dB)	PowerSum TX-RX Xtalk (dB)	PowerSum RX-RX Xtalk (dB)	RX Routing Layers Layers		Comments
-28.63 ¹	-68.9 ³	-43.9 ²	L3, L7	L22, L24	TX middle column routed on L22
-41.2 ³	-54.1 ¹	-43.8 ²	L3, L7	L5, L22, L24	TX middle column routed on L5
-38.6 ³	-55.3 ¹	-44.4 ²	L3, L5	L7, L22, L24	TX middle column routed on L7
-36.7 ²	-63.8 ²	-44.4 ²	L3, L5	L9, L22, L24	TX middle column routed on L9
-36.7 ²	-64.7 ²	-44.4 ²	L3, L5	L9, L22, L24	TX <i>middle</i> column routed on L9 with layer mis registration core L6/L7 – 4 mils

Table 3: Simulated Power Sum Crosstalk per Via Length

Notes:

1. Not allowed.

2. OK with constraints.

3. Good.

4. TX-TX isolation requirement is 35 dB, allowing for 5 dB TX channel insertion loss delta.

5. TX-RX isolation requirement is 65 dB, allowing for 35 dB maximum RX channel loss.

6. RX-RX isolation requirement is 45 dB, allowing for 15 dB RX insertion loss delta.

The simulated TX-to-TX and RX-to-RX crosstalk amplitudes from individual aggressors with the TX middle column routed on L9 (the fourth entry of Table 3) are shown in the following figure. It can be seen that the crosstalk from the diagonal aggressors is more severe than that from the non-diagonal aggressors. The calculated RX-to-RX power sum crosstalk is 44.4 dB, and the TX-to-TX power sum crosstalk is 36.7 dB.

Figure 17: Simulated TX-to-TX & RX-to-RX Crosstalk with TX Middle Column Routed on L9





Optimal Breakout Layer Assignment for Crosstalk Mitigation

The optimal breakout layer assignment for a triple-triple BGA pin pattern identified per the sweep analysis is depicted in the following figure.

- TX port: L9 (middle column), L22, L24
- RX port: L3, L5



Figure 18: **Breakout Layer Assignment for Triple-Triple BGA Pin Pattern**

The simulated worst-case RX-to-RX crosstalk profiles, including calculated power sum crosstalk from all the aggressors based on the optimal breakout layer assignment, are shown in the following table and figure.

Quad	Channel	Routing Layer	Via Length (mil)
210	RX3	L3	8.6
211	RX0	L3	8.6
	RX1	L5	17.3
	RX2	L3	8.6
	RX3	L3	8.6
212	RX0	L5	17.3
	RX1	L3	8.6

Table 4: RX Routing



Figure 19: Simulated RX-to-RX Crosstalk Based on Optimal Breakout Layer Assignment



Similarly, the simulated worst-case TX-to-TX crosstalk profiles, including calculated power sum crosstalk from all the aggressors based on the optimal breakout layer assignment, are shown in the following table and figure.

Quad	Channel	Routing Layer	Via Length (mil)
210	TX3	L9	34.6
211	TX0	L22	102.4
	TX1	L24	111.0
	TX2	L9	34.6
	TX3	L22	102.4
212	TX0	L24	111.0
	TX1	L9	34.6

Table 5: **TX Routing**



Figure 20: Simulated TX-to-TX Crosstalk Based on Optimal Breakout Layer Assignment



Note: The calculated power sum crosstalk in Figure 19 and Figure 20 includes all the adjacent aggressors, which is not the case for 112 Gbps half-density Quad.

Crosstalk Analysis for 112 Gbps Half-density (2 × GT) Quad Usage

As mentioned in TX-to-RX Crosstalk Analysis for 56 Gbps Full-density Quad Usage, crosstalk from diagonal aggressors is more severe than that from non-diagonal aggressors. Both TX-to-TX and RX-to-RX crosstalk can be limited to one diagonal aggressor by deliberately choosing the active lanes in a Quad, thereby reducing the power sum crosstalk.

The simulated TX-to-TX and RX-to-RX crosstalk amplitudes from individual aggressors for 112 Gbps PAM4 (at 28 GHz) based on the optimal breakout layer assignment are shown in the following figure and table.



Figure 21: Simulated TX-to-TX & RX-to-RX Crosstalk Amplitudes at 28 GHz for 112 Gbps





-42.7

-35.1

-55.4

-100.9

-58.4

-65.1

			•	•
GM Dual Chappels		Xtalk @ 112G PAM4, dB		
Givi Dua	r channels	RX-to-RX	TX-to-TX	TX-to-RX
211_CH0	211_CH2	-43.2	-33.7	-91.5

-44.5

-38.9

-79.5

Table 6: Simulated TX-to-TX and RX-to-RX Crosstalk Amplitudes at 28 GHz for 112 Gbps

C4072 Package PCB Breakout Design Guidance

The recommendations for the C4072 package PCB breakout are summarized as follows.

- TX-to-RX isolation must be carefully considered, especially for LR applications
- RX-to-RX isolation for large IL variations must be carefully considered
- Route TX on lower layers rather than RX to avoid trace-to-via coupling
- Provide ~18 mil separation between RX and TX routing layers

211_CH3

211_CH2

211_CH3

• Place GND vias outside BGA pins to improve RX-to-RX isolation

For a 56 Gbps full-density Quad usage, recommendations are as follows:

• TX-to-TX crosstalk

211_CH0

211_CH1

211_CH1

- Worst-case TX victim: Four diagonal aggressors (plus two non-diagonal aggressors separated by a pair of GND balls)
- Middle column of TX pins routed with via length less than 45 mil
- · Victims with fewer aggressors can have longer vias
- RX-to-RX crosstalk
 - Worst-case RX victim: Four diagonal aggressors (plus two non-diagonal aggressors separated by a pair of GND balls)
 - Projected power sum crosstalk at < 14 GHz = -44 dB
 - Recommended restriction: Insertion loss delta between RX channels: < 14 dB
- TX-to-RX crosstalk
 - For LR RX with 35 dB insertion loss, requirement is 65 dB isolation
 - TX routing layer must be at least 18 mil below lowest RX routing layer

Reference Design

Download the reference design files for this application note from the Adaptive SoC Transceiver IBIS-AMI Model Secure website.



Reference Design Matrix

The following checklist indicates the procedures used for the provided reference design.

Table 7: Reference Design Matrix

Parameter	Description			
General				
Developer name	AMD			
Target devices	Versal Premium, Prime, and HBM series			
Source code provided?	Y			
Source code format (if provided)	IBIS-AMI model			
Design uses code or IP from existing reference design, application note, third party or AMD Vivado™ software? If yes, list.	Ν			
Simulation				
Functional simulation performed	Ν			
Timing simulation performed?	Ν			
Test bench provided for functional and timing simulation?	Ν			
Test bench format	N/A			
Simulator software and version	Ansys Electronics Desktop, Keysight ADS			
SPICE/IBIS simulations	Y			
Implementation				
Implementation software tool(s) and version	N/A			
Static timing analysis performed?	Ν			
Hardware Verification				
Hardware verified?	Y			
Platform used for verification	VPK180			

Conclusion

This application note reviews the 112 Gbps PAM4 design challenges and the various impairments on the PCB channel. It specifies the Versal device GTM transceiver PCB channel design requirements in terms of channel insertion loss, return loss, crosstalk, and intra-pair skew. The application note also demonstrates good practices for minimizing and mitigating various impairments and fulfilling the corresponding channel design requirements.

References

These documents provide supplemental material useful with this application note:

- 1. Yohan Frans, IEEE Education Session, Overview of ADC-based Wireline Transceiver, CICC 2019
- 2. Geoff Zhang, et al, A Tutorial on PAM4 Signaling for 56G Serial Link Applications, DesignCon 2017



- 3. OIF Common Electrical I/O (CEI) Electrical and Jitter Interoperability agreements: OIF-CEI-04.0
- 4. IEEE standards for Ethernet: IEEE Std 802.3bs-2017, IEEE Std 8023cd-2018, and IEEE Std 802.3ck-2022
- 5. Versal Adaptive SoC GTM Transceivers Architecture Manual (AM017)
- 6. Versal Prime Series Data Sheet: DC and AC Switching Characteristics (DS956)
- 7. Versal Premium Series Data Sheet: DC and AC Switching Characteristics (DS959)
- 8. Versal HBM Series Data Sheet: DC and AC Switching Characteristics (DS960)
- 9. Eben Kunz, et al, Sources and Compensation of Skew in Single-Ended and Differential Interconnects, DesignCon 2014
- 10. Eric Bogatin, et al, New Characterization Technique for Glass-Weave Skew, DesignCon 2016/2017
- 11. Scott McMorrow, et al, The Impact of PCB Laminate Weave on the Electrical Performance of Differential Signaling at Multi-Gigabit Data Rates, DesignCon, 2005
- 12. Jeff Loyer, et al, Fiber Weave Effect: Practical impact Analysis and Mitigation Strategies, DesignCon 2007
- 13. Versal Adaptive SoC Packaging and Pinouts Architecture Manual (AM013)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary	
05/23/2023 Version 1.0		
Initial release.	N/A	

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