PCB Channel Design Guidelines for 112 Gbps GTM Transceivers

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Summary

High-speed data rate transmissions suffer from distortions to the signal imposed by channel response. 112 Gbps continues to push channel design considerations, both at the board level and in the transceiver. The small unit interval of the symbol combined with the reduced eye amplitude of the 4-level pulse amplitude modulation (PAM4) scheme results in less available budget for impairments, such as crosstalk and jitter. This application note details printed circuit board (PCB) channel design requirements for high-speed serial data transmission, including rates of 56 Gbps and 112 Gbps. Good practices for minimizing and mitigating the various impairments on the PCB are also presented.

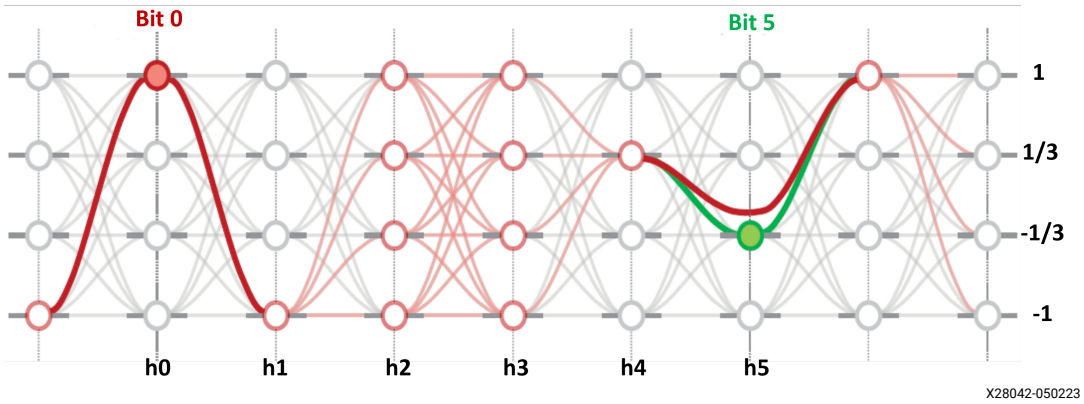
Download the reference design files for this application note from the Versal ACAP Transceiver IBIS-AMI Model Secure website. For detailed information about the design files, see Reference Design.

Introduction

When data rates approach 56 Gbps per lane, a more bandwidth-efficient modulation scheme (PAM4) is deployed. However, PAM4 signaling is susceptible to noise, including intersymbol interference (ISI) and crosstalk, because the eye height is reduced while still generating full amplitude signal swings. The result is the potential worst-case condition of the signal aggressor having a full height voltage transition, while the victim simultaneously has a swing of 1/3 the full height.

As shown in the following figure, taken from Overview of ADC-based Wireline Transceiver [1], suppose the designed channel has 10% reflection at the fifth cursor *h5*, the amplitude of *Bit 5* (green waveform) is h (minor transition from 1/3 to –1/3). For a major transition *Bit 0* (from –1 to 1) with amplitude of $3 \times h$ occurs at cursor *h0* (red waveform), the amplitude of the reflected signal at the fifth cursor *h5* is $0.3 \times h$ ($10\% \times 3 \times h$), which is 30% of *Bit 5*'s amplitude h. The impact of the residual ISI on PAM4 is three times its non-return-to-zero (NRZ) counterpart.

Figure 1: **PAM4 Challenges**



As data rates increase further to 112 Gbps, the unit interval is less than 20 picoseconds. Large numbers of DFE or FFE taps at the RX side are required to manage the multiple reflections from discontinuities that show up far away from the main cursor. *A Tutorial on PAM4 Signaling for 56G Serial Link Applications* [2] provides a thorough review of PAM4 signaling.

The small unit interval combined with PAM4 modulation reduces channel design budget to the point where each element in the channel matters. Besides meeting the channel insertion loss budget, dedicated design efforts should be taken to minimize impedance discontinuity, crosstalk, and skew on the channel.

High-speed data rate transmissions suffer from distortions to the signal imposed by channel response. The most significant impairments from the passive channel include:

- Frequency-dependent attenuation and dispersion from conductor loss and dielectric loss lead to insertion loss (IL).
- Reflections/multiple reflections from discontinuities and impedance mismatch lead to return loss/effective return loss (RL/ERL).
- Crosstalk due to unwanted horizontal coupling and vertical coupling lead to power sum crosstalk (PSXT), insertion loss to crosstalk ratios (ICR), and integrated crosstalk noise (ICN).
- Intra-pair skews originating from asymmetry structure, glass weave, and trace length mismatch lead to mode conversion (SDC/SCD).

The GTM transceiver in the AMD Versal™ adaptive SoC is a dual-mode, multi-protocol transceiver supporting multiple electrical standards, including OIF CEI-56G-VSR/MR/LR [3], and IEEE 802.3bs/cd/ck [4]. It addresses both in-box and out-of-box interconnects, from short reach to long reach (LR) chip-to-chip interfaces within the PCB and across the PCB through board-to-board connecters or direct attached cables (DAC), optical interfaces through pluggable optical modules, or the emerging technology of on-board optics/near-package optics [5].

This application note details the requirements and good practices for minimizing and mitigating various impairments and achieving successful 112 Gbps high-speed serial link designs. These requirements are provided with the channel requirements of any supported protocol. Supported protocols are listed in the datasheets for the Versal devices with GTM transceivers.

- *Versal Prime Series Data Sheet: DC and AC Switching Characteristics* (DS956)

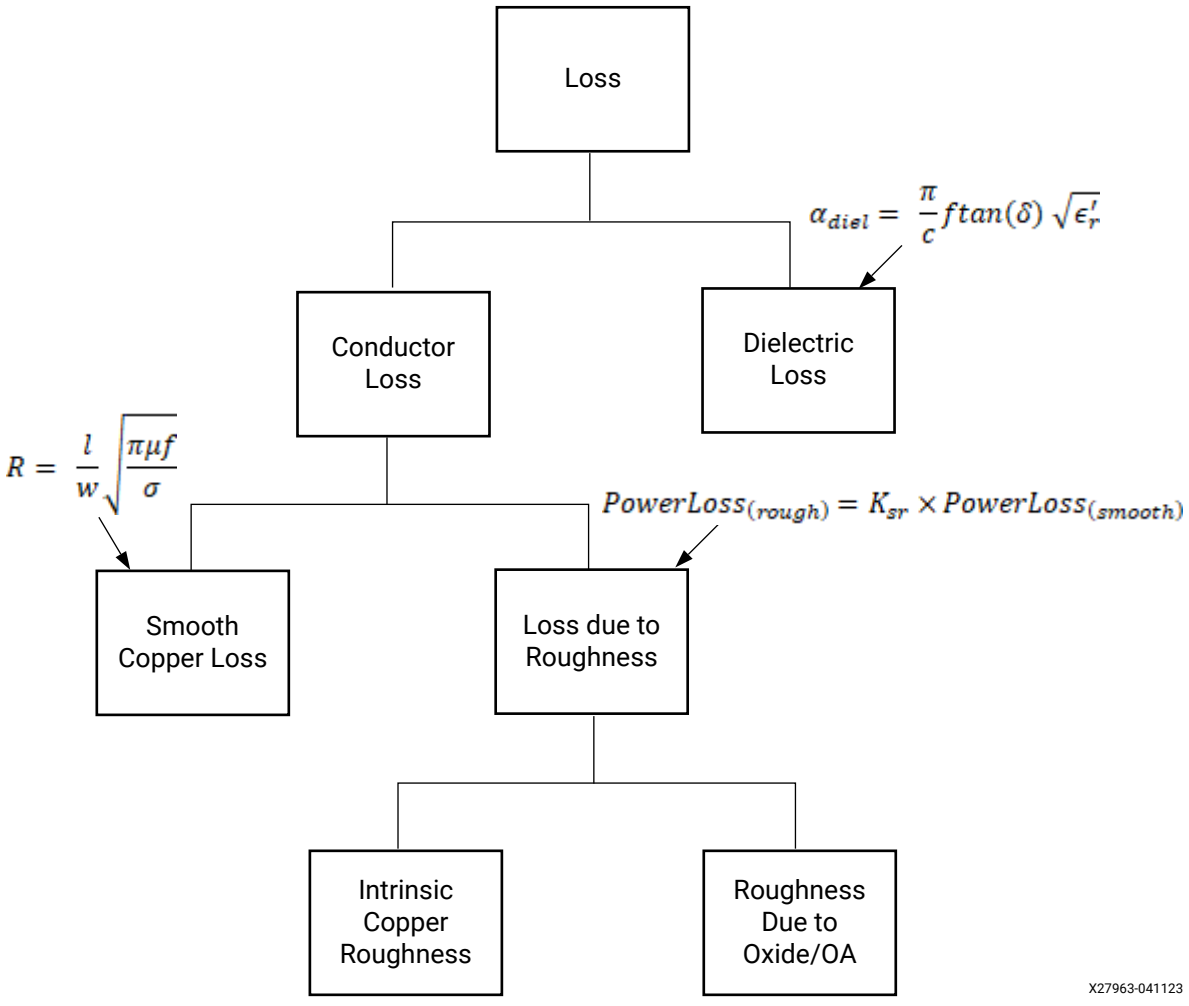
- *Versal Premium Series Data Sheet: DC and AC Switching Characteristics* (DS959)
- *Versal HBM Series Data Sheet: DC and AC Switching Characteristics* (DS960)

Channel Insertion Loss

One ultimate challenge for 112 Gbps electrical interfaces is achieving the desired physical reach while still meeting the constraints of power consumption and bandwidth-limited channels. High-speed data rate transmissions suffer from the frequency-dependent attenuation and dispersion induced by PCB-based or electrical cable-based interconnects.

As illustrated in the following figure, frequency-dependent attenuation and dispersion arise from frequency-dependent conductor loss and dielectric loss, where conductor loss can be subdivided into smooth copper loss due to skin effects and additional loss due to a rough conductor surface. While the die bump-to-die bump channel insertion loss budget is around 35 dB for long reach applications in each generation from 25 Gbps to 100 Gbps, low-loss PCB material, smoother copper with advanced surface treatments, and/or wider traces are required to fulfill the IL budget in the 100 Gbps era.

Figure 2: **PCB Material Loss Decomposition**



The designed channel must meet the recommended maximum and minimum channel insertion loss stipulated in corresponding electrical standards. When paired with a long reach-capable transceiver, the Versal device GTM transceiver can support up to 30 dB ball-to-ball loss (refer to the corresponding standards for the maximum channel IL budgets) at Nyquist (14 GHz for 56 Gbps PAM4 or 28 GHz for 112 Gbps PAM4) with Reed-Solomon (544, 514) Forward Error Correction (RS (544, 514) FEC).

The maximum IL a Versal device GTM transceiver can support also depends on the channel characteristics like discontinues and crosstalk. The designed channel should be evaluated with the channel compliance methods stipulated in the corresponding standard to verify the conformance.

IMPORTANT! *The recommended channel insertion loss requirement (Nyquist = 14 GHz / 28 GHz) is as follows:*

PCB differential insertion loss (@ ≤ Nyquist) from ball-to-ball: ≤ 30 dB

- Insertion loss deviation range 1 [@ ≤ Nyquist]: ≤ ±0.5 dB
- Insertion loss deviation range 2 [@ Nyquist ≤ F ≤ (1.5 x Nyquist)]: ≤ ±1.0 dB

Impedance Discontinuity

Impedance discontinuity causes energy reflection. With the presence of an impedance discontinuity in the transmission path, part of the transmitted signal reflects back to the transmitter and is not detected by the receiver. Each discontinuity reduces the amount of signal that is delivered to the receiver. In addition, multiple reflections distort the forward propagating waveform. Common sources of discontinuities include package-to-PCB interfaces, PCB vias, surface-mount device (SMD) footprints, connectors, and cable-to-connector interfaces.

Via Impedance Optimization

- PCB vias are a source of impedance discontinuities if not properly designed. The via stub, antipad size, drill hole size, and differential via pitch are important features for via impedance control.
- Minimizing via stub is crucial for securing 112 Gbps channel designs. A via stub can cause a ¼ wave resonance. At the resonance frequency, a deep notch appears on the insertion loss due to the cancellation between the 180-degree out-of-phased reflected signal from the stub and the transmitting signal. The resonance frequency can be estimated as follows.

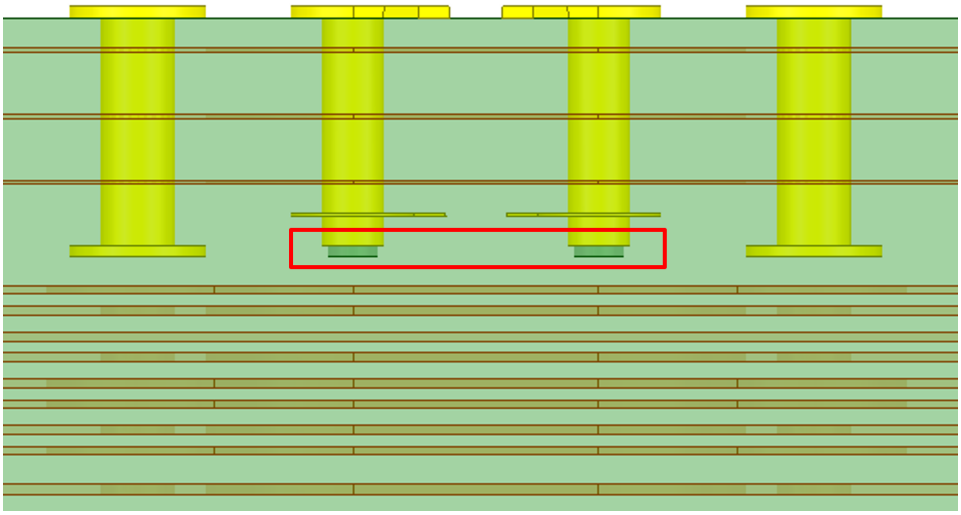
Equation 1: **¼ Wave Resonance Frequency**

$$f_{res} = \frac{c}{4 \times l \times \sqrt{Dk_{eff}}}$$

Where f_{res} is the ¼ wave resonance frequency, c is the speed of light in vacuum, l is the stub length, and Dk_{eff} is the effective dielectric constant the via sees. Dk_{eff} is normally higher than the PCB dielectric material's dielectric constant because of the coupling between via barrel/pads and the reference planes surrounding the via. To minimize the impact of the ¼ wave resonance on the signal, it is recommended to push the resonance frequency well above the signal bandwidth, for example, > 2 × signal bandwidth.

- The most common way to match via impedance with channel nominal impedance is tuning the via antipad size to adjust the capacitance and inductance ratio. However, a small via antipad is preferred in the ball grid array (BGA) pin field to reduce the trace-via crosstalk. For the BGA via impedance optimization, return loss and crosstalk should be evaluated simultaneously to determine the optimal point for maximal system margin.
- For the blind via, extending the antipad void to the layers beneath the via mitigates the excess capacitance from the coupling between the via pad and the planes. For a blind via with a lead-out trace not routed on the bottom layer of the via, for example a blind via in sequential lamination, removing the via bottom layer pad like a landless via helps with minimizing the capacitance as well, as shown in the following figure.

Figure 3: **Landless Blind Via**



- Unlike the 25 Gbps NRZ / 56 Gbps PAM4 channel where an identical antipad on all the layers is sufficient for optimal via impedances in the frequency band of interest, tuning the antipad size/shape per layer is necessary to keep a low return loss for the wider frequency band in 112 Gbps designs.
  - The antipad voids on the stripline reference plane layers have a significant impact because of the excess inductance from the lead-in/out trace losing its reference in the void range.
  - The antipad void on layer 2 has a significant impact because of capacitive coupling to the top layer pad.
- Spacing of the signal and GND vias has a significant impact. Outside the BGA pin field, the GND vias should be placed as close to the signal via as possible, but not encroach into the signal via antipad void range. In the BGA pin field, the placement of GND vias should follow the pattern of GND balls.

SMD Footprint Optimization

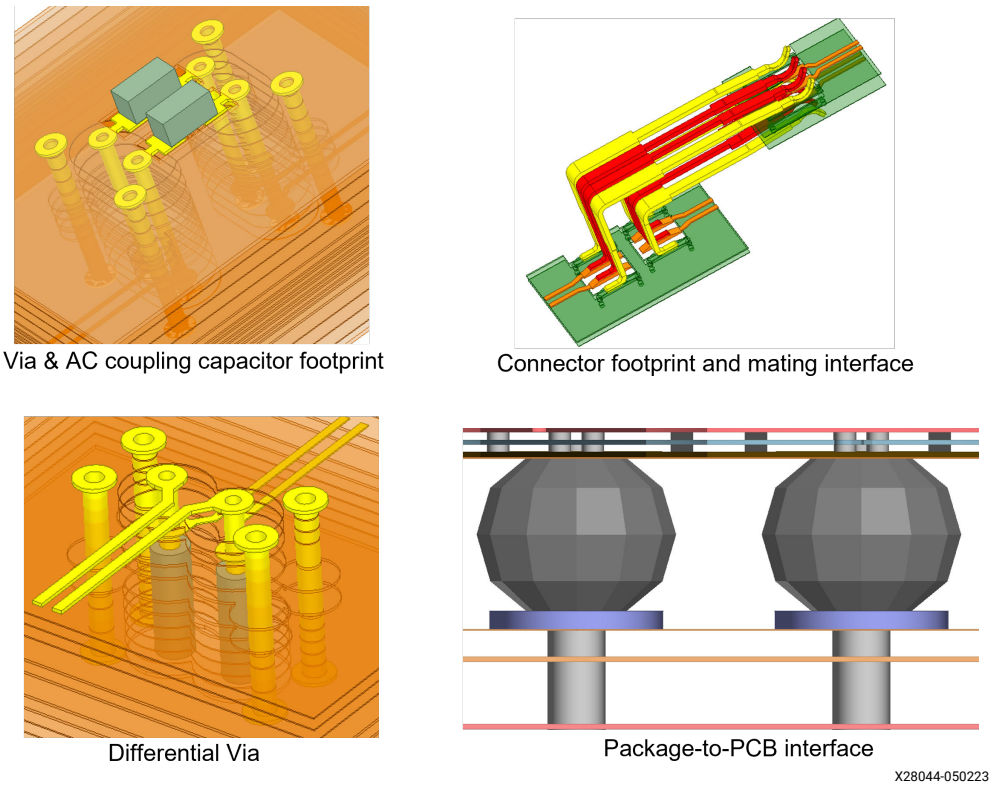
- Another significant discontinuity on the link is the footprint of the SMD, such as AC coupling capacitors, board-to-board connectors, and BGA pads.

- Generally, the footprints show excess capacitance with the combination of dielectric thickness to the reference plane and footprint geometries. Thus, the reference plane beneath the SMD pads should be voided to remove the capacitance.
- Both an optimal cut-out depth and cut-out size (width, length, and radius) that minimize the return loss of the structure should be identified.

Optimal Channel Nominal Impedance

- When there are large discontinuities that cannot be eliminated, the optimal trace impedance should be determined in a way that minimizes the multiple reflections from the discontinuities. It is not necessary to adhere to 100Ω or 85Ω.
- The nominal trace impedance of the Versal device GTM transceiver channel package is 92 ~ 93Ω ± 10%.
- The channel nominal impedance should be selected per system-level SI analysis with all discontinuities included.

Figure 4: **Discontinuity Examples**



As illustrated in the previous figure, discontinuities usually occur at vertical transition regions, like package-to-PCB interfaces and PCB-to-connector interfaces. Attention to detail at every signal transition region is critical to achieve a successful 112G channel design.

IMPORTANT! *The recommended channel return loss requirement is as follows:*

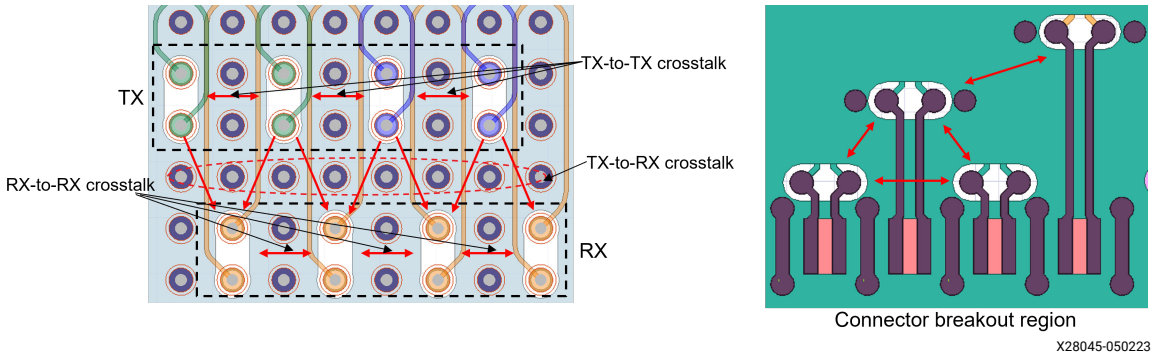
- PCB differential return loss (@ ≤ Nyquist): ≤ –12 dB [at the solder ball]
- PCB common-mode return loss (@ ≤ Nyquist): ≤ –15 dB

- PCB differential-to-common mode return loss (@ all frequencies): ≤ –15 dB
- PCB common-to-differential mode return loss (@ all frequencies): ≤ –15 dB

Crosstalk

Crosstalk is unwanted coupling between aggressor signals and victim signals, which can happen anywhere throughout the link. Common sources of crosstalk are connectors, BGA vias, PCB/package traces, cables, AC coupling capacitors and accompanying vias. In all cases, crosstalk is a function of the relative signal strength of the aggressor versus the victim at the region of coupling. For instance, if the victim is a receive channel that has incurred 30 dB of attenuation, and the aggressor is a nearby transmitter that has yet to encounter any attenuation, the crosstalk isolation must account for the strength of the aggressor. In this example, if the aggressor is 30 dB stronger than the victim, the crosstalk isolation must include at least 30 dB of isolation to counteract the aggressor signal strength. Because crosstalk is dependent on the relative strength of the victim and the aggressor, crosstalk isolation is especially important when adjacent channels have very different insertion loss profiles.

Figure 5: **Crosstalk Examples**



IMPORTANT! *The recommended channel crosstalk requirement is as follows:*

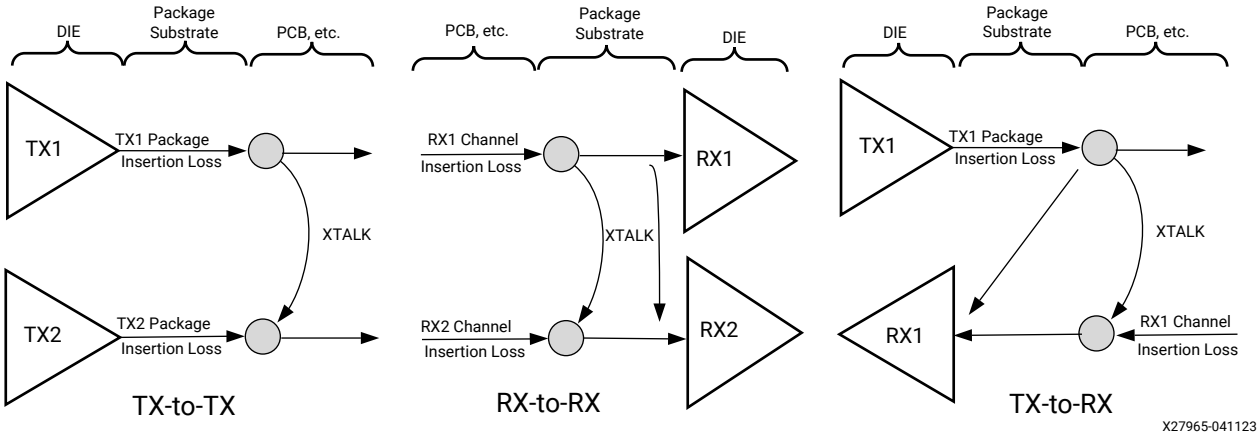
- Worst-case signal to power sum crosstalk ratio (IL roll-off with frequency, crosstalk flat or ramp-up with frequency) up to Nyquist frequency for NRZ application ≥ 20 dB
- Worst-case signal to power sum crosstalk ratio up to Nyquist frequency for PAM4 application ≥ 30 dB due to ~10 dB signal-to-noise ratio (SNR) lost by splitting one eye in NRZ into three in PAM4 (aggressor full swing – victim 1/3 full swing)

As illustrated in the following figure, within the BGA pin field there are three types of crosstalk:

- **TX-TX Coupling:** This type of coupling is not influenced by the channel loss because the signal has yet to encounter the channel. Therefore, the crosstalk isolation required is independent of the channel loss for either the victim or aggressor.

- **RX-RX Coupling:** An important factor in calculating the required crosstalk isolation is the relative insertion loss of the victim and aggressor channels. If the victim channel is an LR channel with 30 dB of insertion loss and the aggressor is a short reach channel with only 10 dB of insertion loss, the crosstalk isolation must include attenuation of 20 dB to account for the difference between the aggressor and victim signal strength. Because of this, it is important to identify cases in the application where there is a disparity between the insertion loss of the victim and the aggressor.
- **TX-RX Coupling:** The TX incurs little attenuation while the attenuation of the RX can vary significantly. This type of crosstalk coupling is very dependent on insertion loss in the RX channel and is independent of the channel loss in the TX channel. The greater the loss in the RX channel, the more crosstalk isolation is required between the TX and RX. This coupling does not depend on the type of channel like LR and very short reach (VSR) for TX as is the case for TX-TX coupling. Instead, it is completely dependent on the RX channel insertion loss. More channel insertion loss requires more crosstalk isolation.

Figure 6: **Crosstalk Components**



The crosstalk isolation requirement is a function of the assigned crosstalk allowed in the channel link impairment budget, the victim, and the relative strength of the victim and the aggressor. For NRZ signaling, the type of coupling is used to define the relative strength of the victim and the aggressor. For PAM4 signaling, an additional 10 dB of isolation is required to cover the case when the aggressor signal swing is full amplitude and the victim swing is only 1/3 of that amplitude. So, for PAM4 signaling, if the budget for the crosstalk component is 10%, the crosstalk isolation for all types of coupling would be 30 dB. The isolation due to the type of coupling, TX-TX, RX-RX, or TX-RX, is added. See the following table for examples of crosstalk targets for various interface boundary conditions.

Table 1: **Examples of Isolation Targets for Various Interface Boundary Conditions**

Protocol Interface Boundary	Victim[3] Insertion Loss		Aggressor[3] Insertion Loss		Budget[1] (dB)	PAM4[2] (dB)	Minimum Isolation Target Power Sum for PAM4[4] (dB)			Minimum Isolation Target Power Sum for NRZ[5] (dB)		
	RX (dB)	TX (dB)	RX (dB)	TX (dB)			RX-RX	TX-RX	TX-TX	RX-RX	TX-RX	TX-TX
VSR-LR	35	5	10	0	20	10	55	65	35	45	55	25
VSR-VSR	15	5	5	0	20	10	40	45	35	30	35	25

Table 1: **Examples of Isolation Targets for Various Interface Boundary Conditions** *(cont'd)*

Protocol Interface Boundary	Victim[3] Insertion Loss		Aggressor[3] Insertion Loss		Budget[1] (dB)	PAM4[2] (dB)	Minimum Isolation Target Power Sum for PAM4[4] (dB)			Minimum Isolation Target Power Sum for NRZ[5] (dB)		
	RX (dB)	TX (dB)	RX (dB)	TX (dB)			RX-RX	TX-RX	TX-TX	RX-RX	TX-RX	TX-TX
LR-LR	35	5	23	0	20	10	42	65	35	32	55	25

Notes:

1. Allow 10% of eye for crosstalk component.
2. Reduce eye to one third of full signal swing for PAM4 signaling.
3. Loss applied to signal for signal amplitude at BGA ball.
4. Min Isolation Target for PAM4 = Budget + PAM4 + VictimIL – Aggressor IL.
5. Min Isolation Target for NRZ = Budget + Victim IL – Aggressor IL.

The reason that the BGA pin field is usually a high crosstalk region is the via-via and trace-via coupling. The breakout layer should be assigned in a way that minimizes the via-via and trace-via coupling. Some good practices for minimizing the crosstalk in a BGA pin field are as follows:

- A shallow breakout layer with a short via barrel and thus small vertical parallelism is preferred to minimize via-via coupling.
- If a long via barrel must be used, staggering the routing layers of adjacent pairs is a good practice to reduce via vertical parallelism.
- Route inner pairs on lower layers rather than outer pairs to avoid trace-via coupling.
- Place GND vias along the BGA field edge to improve isolation for pairs at the edge of the ball array.

IMPORTANT! *The recommended channel crosstalk requirement for the BGA PCB breakout region for PAM4 signaling is as follows:*

- Worst-case differential TX power sum of all aggressors to victim TX: < –35 dB up to Nyquist frequency
- Worst-case differential RX power sum of all aggressors to victim RX: < –55 dB up to Nyquist frequency
- Worst-case differential TX power sum of all aggressors to victim RX: < –65 dB up to Nyquist frequency

Intra-pair Skew

The skew between the two legs of a differential pair causes differential signal to common mode signal conversion as well as reverse mode conversion. Mode conversion distorts the differential signal and thus creates a reduced differential signal. A common mode signal might re-convert back into a differential signal, creating increased differential noise. Some common sources of skew are asymmetrical structures from manufacturing variations or unintentional return path asymmetry, glass weave, and trace length mismatch. In *Sources and Compensation of Skew in Single-Ended and Differential Interconnects* [9], you will find a review of various sources of intra-pair skews.

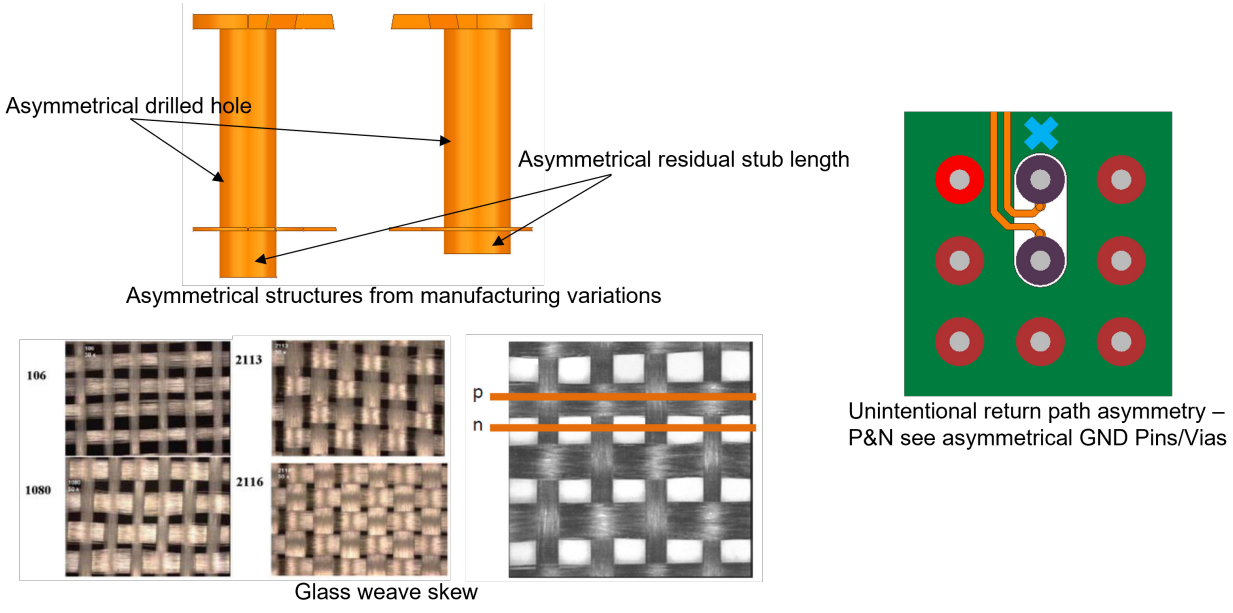
Intra-pair Trace Length Matching

- The differential signal and common mode signal in a microstrip or via have different propagation velocities due to the different effective dielectric constants of the surrounding materials seen by the signals.
- The propagation velocities of the differential signal and common mode signal differ in an inhomogeneous stripline because the core and pre-preg around the signal conductors have different dielectric constants and loss tangents. There are also different spatial distributions of resin and glass weave around the signal/GND conductors.
- Due to the different propagation velocity for the two modes, the skew on a microstrip should be compensated just after where the skew occurs, similar to an inhomogeneous stripine. Eliminating length compensation by routing bend/turning with arcs is preferred rather than compensating the skew with a single big loop or several small serpentines.
- Similarly, due to the different propagation velocity in a via, the skew should be compensated before a trace enters the via, even if both ends of the via are stripline with a similar dielectric constant. That is, the skew compensation should be made on the same layer as where the skew occurs.
- The skew on a homogeneous stripline can be compensated with reversed (mirrored) bends, a single big loop, or several small serpentines. When compensating skew with serpentines, maintain sufficient spacing between adjacent legs to avoid self-coupling between the segments. The goal is to maintain the impedance and validate the compensation structure with simulation.

One significant contributor to mode conversion is glass weave skew. Resin and woven glass fibers have different electrical properties in terms of dielectric constants and loss tangents. When one leg of a differential pair is routed on resin and the other is routed on glass fiber, skew is generated due to different propagation velocities. There has been significant industry research in this area that characterizes the impact of glass weave and identifies methods to mitigate its effect [10, 11, and 12]. Some commonly used methods to mitigate the weave skew effect are listed below. Appropriate methods should be picked based on the balance between cost and implementation effort to minimize the glass weave skew effect.

- Angled or zig-zag routing
- Jagged routing per differential pair pitch
- Rotating the panel
- Matching differential pair pitch to weave pitch
- Multi-ply with different weave pitches
- Advanced weave, for example, glass fiber with low dielectric constant (closer to the resin dielectric constant), tighter weave

Figure 7: **Intra-pair Skew Examples**



IMPORTANT! *Recommended intra-pair skew for a PCB design is < 1 ps.*

System-Level SI Analysis

The Versal device GTM transceiver is designed and validated to meet protocols that assume the passive channel and link partner are compliant in all cases. The designed channel must be evaluated with a channel compliance tool or tolerancing test method stipulated in corresponding standards like channel operation margin (COM) for IEEE and OIF CEI to verify the conformance. In addition to channel compliance checks, channel simulation using an IBIS algorithmic modeling interface (IBIS-AMI) model should be run to confirm the final system margin.

Figure 8: **End-to-End Channel Model**

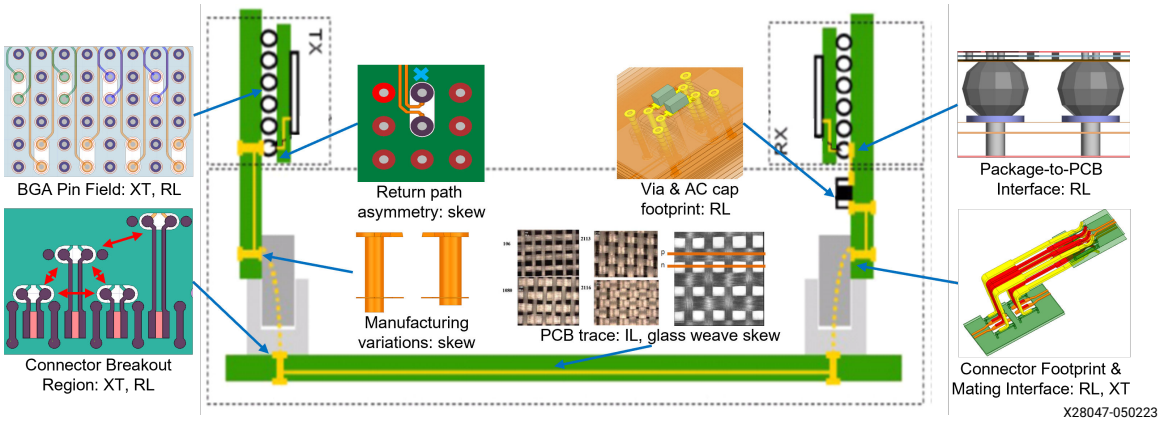


Figure 9: **Channel Compliance Checking with COM**

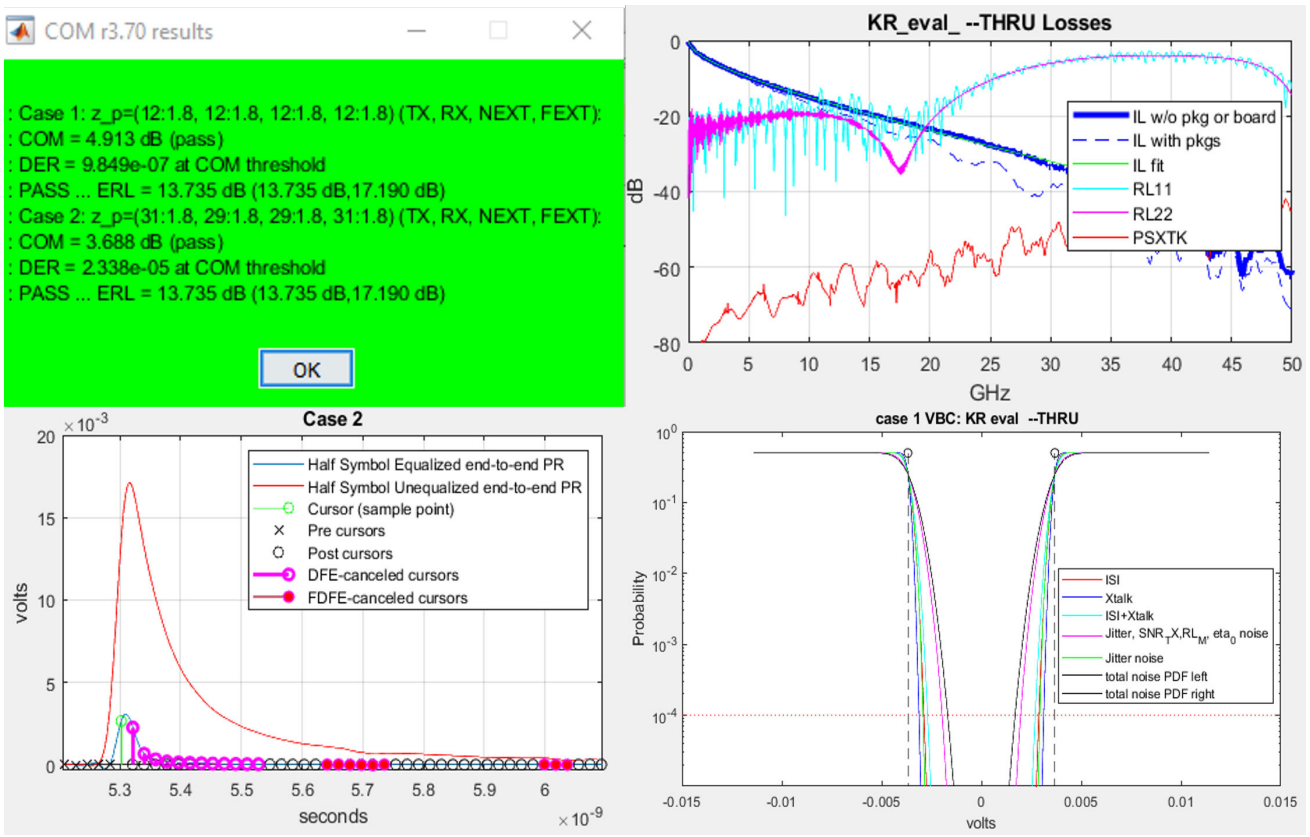
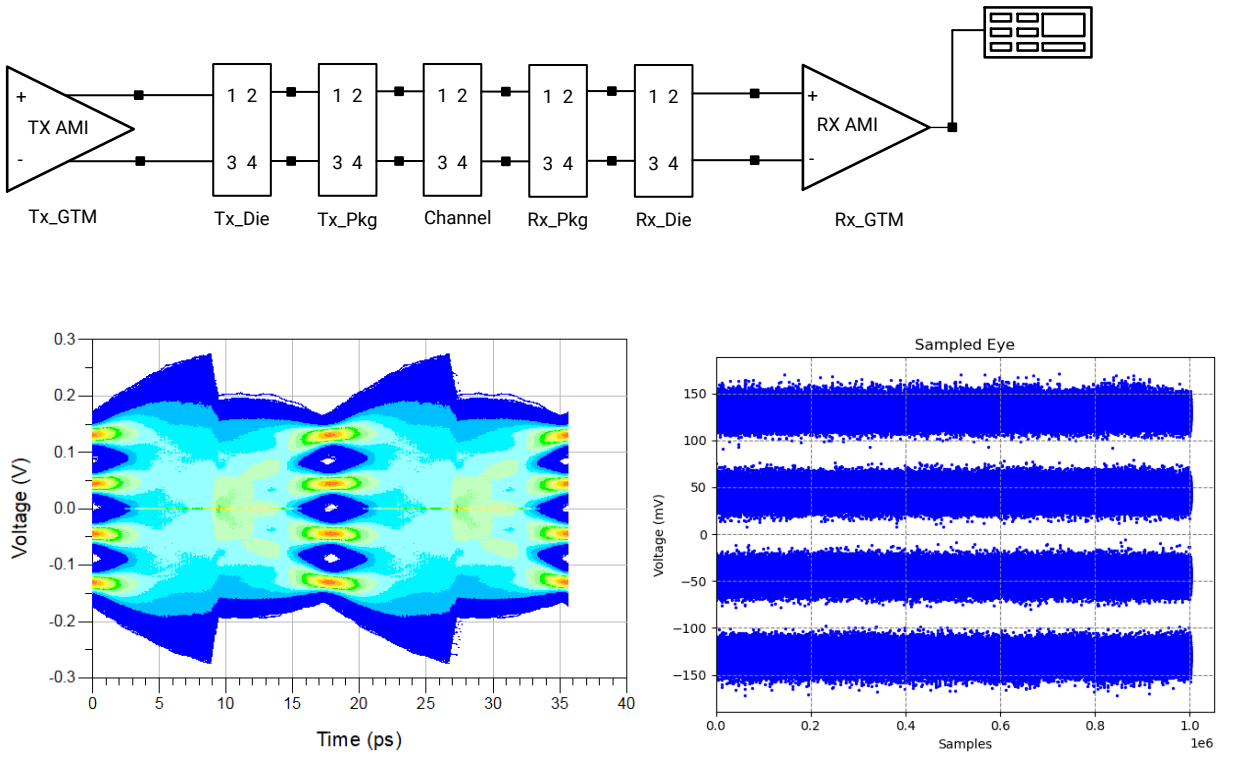


Figure 10: **Channel Simulation with Versal Device GTM Transceiver IBIS-AMI Model**



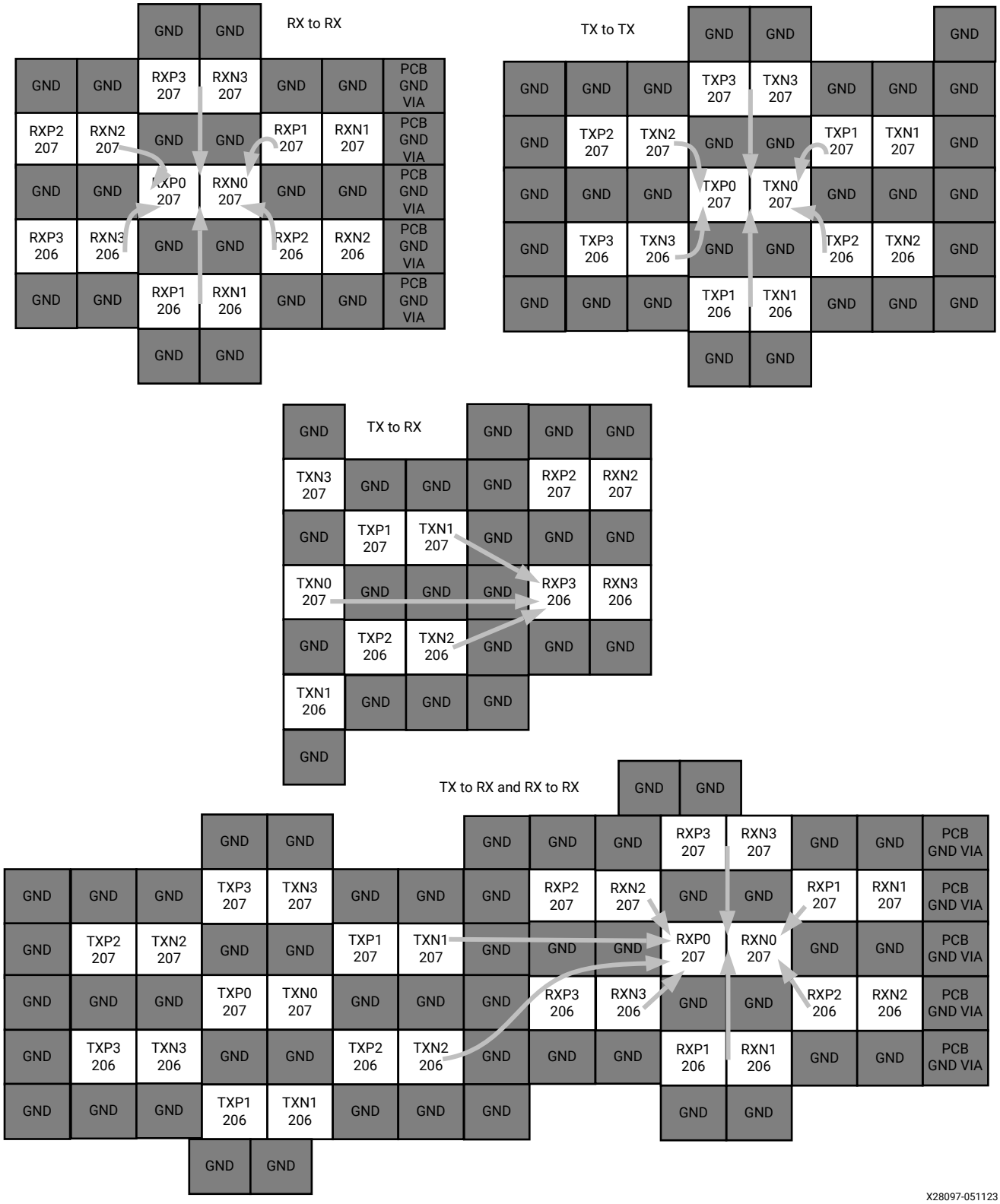
Guidance for C4072 Package PCB Breakout

As mentioned in the Crosstalk section, a BGA pin field is a high crosstalk region due to via-via and trace-via coupling from the limited routing space. This section details important design considerations for the VP1802 C4072 package PCB breakout. These considerations should be carefully studied when using full Versal device GTM transceiver Quads for 56 Gbps LR-LR and VSR-LR reach applications. When using half of the channels in each of the Versal device GTM transceiver Quads, 112 G LR-LR operation is achievable by following the same design considerations. For designs that exceed these guidelines, consider using the A5601 package instead which supports 56 Gbps full-density Versal device GTM transceiver Quad implementation from VSR to LR reaches. See *Versal Adaptive SoC Packaging and Pinouts Architecture Manual* (AM013) for the design considerations regarding the A5601 package.

C4072 BGA Pin Pattern Examples

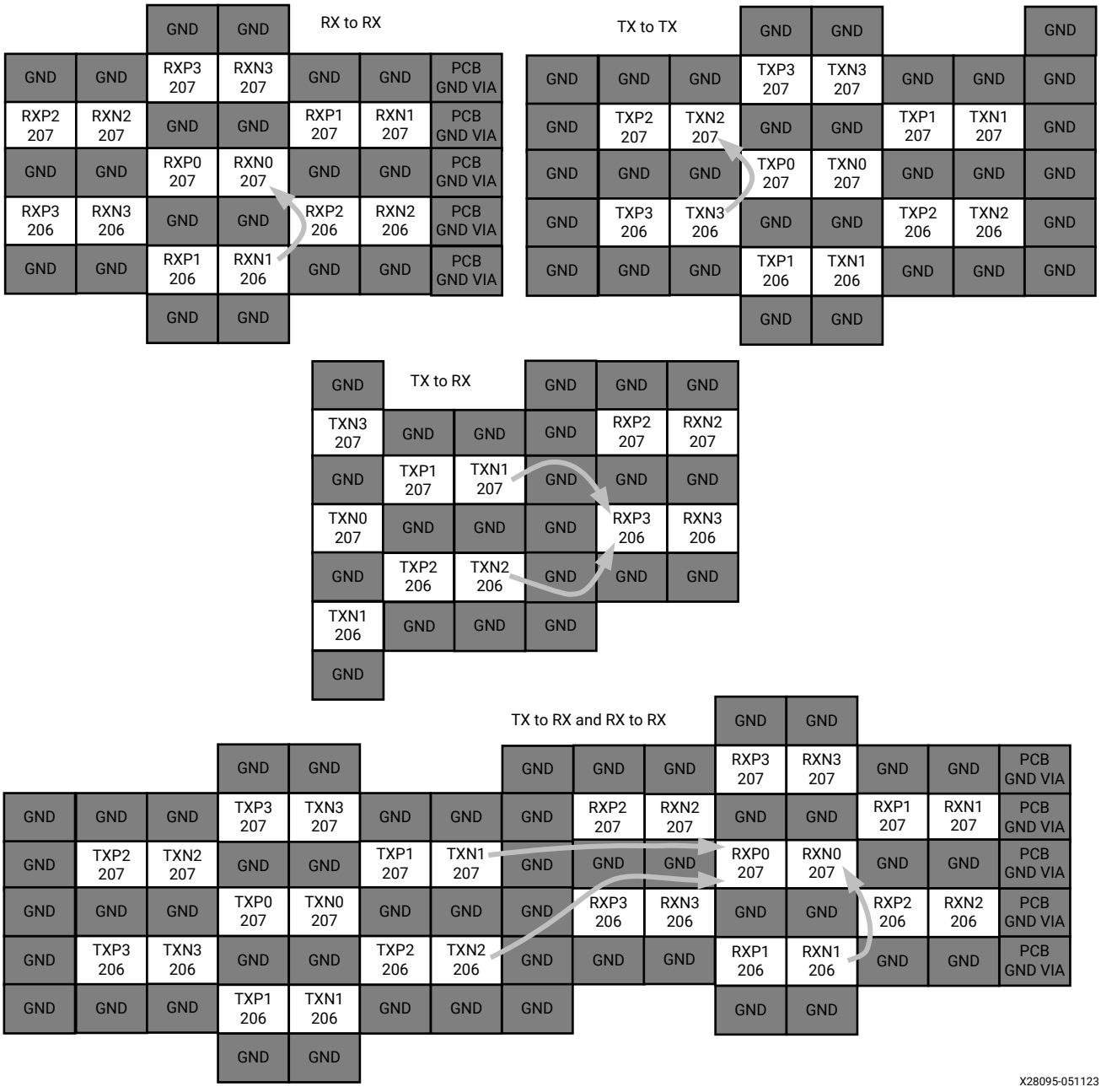
The BGA pin pattern examples for 56 Gbps full-density Quad usage are illustrated in the following figure. As shown in the figure, the RX pairs are located along the periphery of the BGA. TX pairs are located at the interior with one column of GND balls for TX-to-RX isolation. The worst-case victim RX/TX pair is surrounded by four diagonal aggressors plus two non-diagonal aggressors separated by a pair of GND balls. In addition to the RX-to-RX/TX-to-TX crosstalk, the trace-via coupling due to the TX pair lead-out traces routed near the RX pair via barrels can jeopardize the TX-to-RX isolation.

Figure 11: **BGA Pin Pattern Examples – 56 Gbps Quad**



GTM transceivers can operate at data rates up to 112 Gbps by using two out of the four transceivers in each Quad. As illustrated in the following figure, by choosing one of (Lane0 or Lane1) and one of (Lane2 or Lane3) in a Quad, both TX-to-TX and RX-to-RX crosstalk are limited to one diagonal aggressor. Therefore, the minimum isolation targets are easier to achieve without strict layout guidelines.

Figure 12: **BGA Pin Pattern Examples – 112 Gbps Dual**

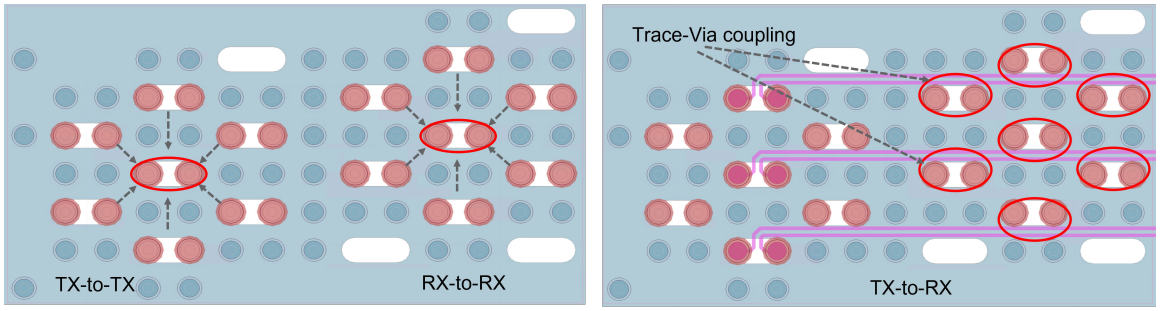


The crosstalk components depicted in Figure 6: Crosstalk Components are listed below and illustrated in the following figure.

- **TX-to-TX coupling:** Dominated by via-via coupling and occurs at BGA pin
- **RX-to-RX coupling:** Dominated by via-via coupling and occurs at BGA pin

- **TX-to-RX coupling:** Dominated by trace-via coupling and occurs at RX BGA pin

Figure 13: **Crosstalk Components in BGA Pin Field**



PCB Stackup and Via Construction for Example PCB Breakout Design

An example PCB breakout design based on the C4072 package is provided to demonstrate good practices regarding BGA breakout optimization for crosstalk mitigation.

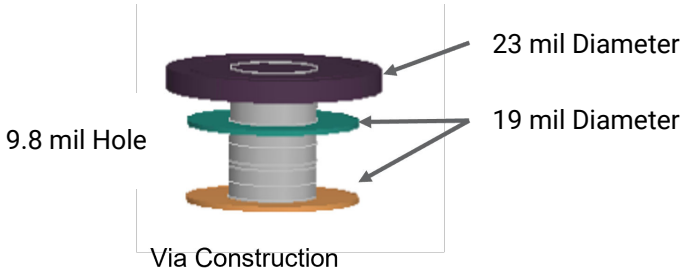
The PCB stackup and via construction used for the analysis are summarized as follows:

- 28-layer stackup with a total thickness of 131.9 mil
- Eight inner signal layers L3, L5, L7, L9, L20, L22, L24, and L26
- Via-in-pad
- EM890K PCB material (1035 × 1035) with HVLP copper foil for signal layers

Figure 14: **28-Layer Reference Stackup**

Material	Name	FillMaterial	Layer Thickness (mils)	Thickness from Top (mils)	Type
SOLDERMASK_LPI_GREEN	UNNAMED_001		0.8		dielectric
.43OZ_PLATED_2PS	TOP	TOP_FILL	2.5	2.5	conductor
001 EM890K 1X1078 RC69 PREG 3P41 DK2P94	UNNAMED_003		3.41	5.91	dielectric
05OZ_HVLP_CU_DK3P26	L2_GND	L2_GND_FILL	0.6	6.51	conductor
002 EM890K 1X1035 RC66 CORE 2P0 DK2P98	UNNAMED_005		4	10.51	dielectric
05OZ_HVLP_CU_DK3P26	L3_MGT01	L3_MGT01_FILL	0.6	11.11	conductor
003 EM890K 1X1035 RC69 PREG 1P735 DK2P94	UNNAMED_008		3.47	14.58	dielectric
05OZ_HVLP_CU_DK3P26	L4_GND	L4_GND_FILL	0.6	15.18	conductor
002 EM890K 1X1035 RC66 CORE 2P0 DK2P98	UNNAMED_011		4	19.18	dielectric
05OZ_HVLP_CU_DK3P26	L5_MGT02	L5_MGT02_FILL	0.6	19.78	conductor
003 EM890K 1X1035 RC69 PREG 1P735 DK2P94	UNNAMED_014		3.47	23.25	dielectric
05OZ_HVLP_CU_DK3P26	L6_GND	L6_GND_FILL	0.6	23.85	conductor
002 EM890K 1X1035 RC66 CORE 2P0 DK2P98	UNNAMED_017		4	27.85	dielectric
05OZ_HVLP_CU_DK3P26	L7_MGT03	L7_MGT03_FILL	0.6	28.45	conductor
003 EM890K 1X1035 RC69 PREG 1P735 DK2P94	UNNAMED_020		3.47	31.92	dielectric
05OZ_HVLP_CU_DK3P26	L8_GND	L8_GND_FILL	0.6	32.52	conductor
002 EM890K 1X1035 RC66 CORE 2P0 DK2P98	UNNAMED_023		4	36.52	dielectric
05OZ_HVLP_CU_DK3P26	L9_MGT04	L9_MGT04_FILL	0.6	37.12	conductor
003 EM890K 1X1035 RC69 PREG 1P735 DK2P94	UNNAMED_026		3.47	40.59	dielectric
1OZ_VLP_CU_DK3P33	L10_1OZ_GND	L10_1OZ_GND_FILL	1.2	41.79	conductor
002 EM890K 1X1035 RC66 CORE 2P0 DK2P98	UNNAMED_029		4	45.79	dielectric
05OZ_HVLP_CU_DK3P26	L11_2OZ_PWR	L11_2OZ_PWR_FILL	0.6	46.39	conductor
003 EM890K 1X1035 RC69 PREG 1P735 DK2P94	UNNAMED_031		3.47	49.86	dielectric
1OZ_VLP_CU_DK3P33	L12_1OZ_GND	L12_1OZ_GND_FILL	2.4	52.26	conductor
009 EM370Z 1X1078 RC58 CORE 2P5 DK3P16	UNNAMED_034		2.5	54.76	dielectric
2OZ_VLP_CU_DK3P33	L13_2OZ_PWR_	L13_2OZ_PWR__FILL	2.4	57.16	conductor
008 EM370Z 1X1060 RC75 PREG 2P03 DK2P94	UNNAMED_036		4.28	61.44	dielectric
2OZ_VLP_CU_DK3P33	L14_2OZ_PWR_CENTER	L14_2OZ_PWR_CENTER_FILL	2.4	63.84	conductor
011 EM370Z 1X1086 RC61 CORE 3P0 DK3P16	UNNAMED_039		3	66.84	dielectric
2OZ_VLP_CU_DK3P33	L15_2OZ_PWR_CENTER	L15_2OZ_PWR_CENTER_FILL	2.4	69.24	conductor
008 EM370Z 1X1060 RC75 PREG 2P03 DK2P94	UNNAMED_041		4.28	73.52	dielectric
2OZ_VLP_CU_DK3P33	L16_2OZ_PWR	L16_2OZ_PWR_FILL	2.4	75.92	conductor
009 EM370Z 1X1078 RC58 CORE 2P5 DK3P16	UNNAMED_044		2.5	78.42	dielectric
1OZ_VLP_CU_DK3P33	L17_1OZ_GND	L17_1OZ_GND_FILL	1.2	79.62	conductor
008 EM370Z 1X1060 RC75 PREG 2P03 DK2P94	UNNAMED_046		4.06	83.68	dielectric
2OZ_VLP_CU_DK3P33	L18_2OZ_PWR	L18_2OZ_PWR_FILL	2.4	86.08	conductor
009 EM370Z 1X1078 RC58 CORE 2P5 DK3P16	UNNAMED_049		2.5	88.58	dielectric
1OZ_VLP_CU_DK3P33	L19_1OZ_GND	L19_1OZ_GND_FILL	1.2	89.78	conductor
006 EM890K 1X1035 RC69 PREG 1P695 DK2P94	UNNAMED_051		3.39	93.17	dielectric
05OZ_HVLP_CU_DK3P26	L20_SIG	L20_SIG_FILL	0.6	93.77	conductor
002 EM890K 1X1035 RC66 CORE 2P0 DK2P98	UNNAMED_054		4	97.77	dielectric
05OZ_HVLP_CU_DK3P26	L21_GND	L21_GND_FILL	0.6	98.37	conductor
003 EM890K 1X1035 RC69 PREG 1P735 DK2P94	UNNAMED_057		3.47	101.84	dielectric
05OZ_HVLP_CU_DK3P26	L22_SIG	L22_SIG_FILL	0.6	102.44	conductor
002 EM890K 1X1035 RC66 CORE 2P0 DK2P98	UNNAMED_060		4	106.44	dielectric
05OZ_HVLP_CU_DK3P26	L23_GND	L23_GND_FILL	0.6	107.04	conductor
003 EM890K 1X1035 RC69 PREG 1P735 DK2P94	UNNAMED_063		3.47	110.51	dielectric
05OZ_HVLP_CU_DK3P26	L24_SIG	L24_SIG_FILL	0.6	111.11	conductor
002 EM890K 1X1035 RC66 CORE 2P0 DK2P98	UNNAMED_066		4	115.11	dielectric
05OZ_HVLP_CU_DK3P26	L25_GND	L25_GND_FILL	0.6	115.71	conductor
003 EM890K 1X1035 RC69 PREG 1P735 DK2P94	UNNAMED_069		3.47	119.18	dielectric
05OZ_HVLP_CU_DK3P26	L26_SIG	L26_SIG_FILL	0.6	119.78	conductor
002 EM890K 1X1035 RC66 CORE 2P0 DK2P98	UNNAMED_072		4	123.78	dielectric
05OZ_HVLP_CU_DK3P26	L27_GND	L27_GND_FILL	0.6	124.38	conductor
001 EM890K 1X1078 RC69 PREG 3P41 DK2P94	UNNAMED_075		3.41	127.79	dielectric
.43OZ_PLATED_2PS	BOTTOM	SOLDERMASK_LPI_GREEN_1	2.5	130.29	conductor
SOLDERMASK_LPI_GREEN_1	UNNAMED_077		0.8	131.09	dielectric
		Total PCB Thickness	131.89		

Figure 15: **Via Construction**



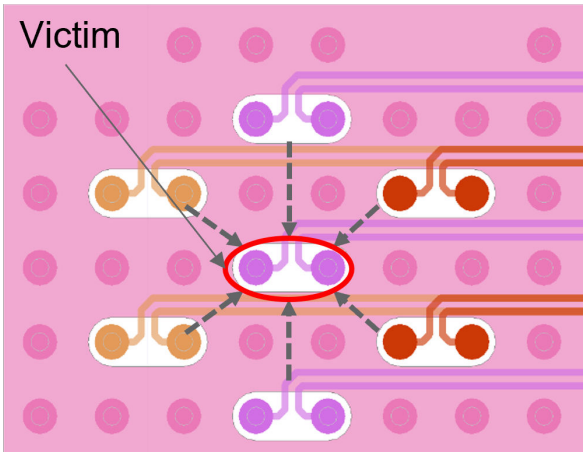
- L1-L3 Stacked MicroVila
- L1-L5 Backdrilled
- L1-L7 Backdrilled
- L1-L9 Backdrilled
- L1-L22 Backdrilled
- L1-L24 Backdrilled
- Backdrilled Stub Length ~=5 mils

X28049-050223

TX-to-TX/RX-to-RX Crosstalk Analysis for 56 Gbps Full-density Quad Usage

As shown in the following figure, the worst-case victim is in the middle column with four diagonal and two non-diagonal aggressors. The routing layers (via length) for the victim in the middle column and the two diagonal aggressors to the right of the victim are swept to visualize the effects of the via vertical parallelism to the crosstalk. The routing layer of the two diagonal aggressors to the left of the victim is kept to L24 (long vias) in the sweep analysis.

Figure 16: **Victim with Four Diagonal and Two Non-Diagonal Aggressors**



X28050-050223

The following table lists the simulated power sum crosstalk for 56 Gbps PAM4 (at 14 GHz) for various routing cases. The data shows that the crosstalk amplitude correlates with the via vertical coupling length between victim and aggressors. A victim with four diagonal aggressors needs a via length < 45 mil to fulfill the –35 dB TX-to-TX power sum crosstalk requirement as stipulated in Table 1.

Table 2: **Simulated TX-to-TX Power Sum Crosstalk per Via Length**

Powersum TX Xtalk (dB)	Victim Via Length (mil)	Aggressor Left Layer	Victim Center Layer	Aggressor Right Layer	Comments
–28.7[1]	102.3	L24	L22	L22	Routed two layers (L22 and L24) long vias
–28.9[1]	102.3	L24	L22	L20	Routed three layers (L20, L22, and L24) long vias
–34.6[1]	44.1	L24	L11	L11	Routed two layers (L11 and L24) short vias
–34.0[1]	54.6	L24	L13	L11	Routed three layers (L11, L13, and L24) short vias
–34.5[1]	44.1	L24	L11	L22	Routed three layers (L11, L22, and L24) short vias
–35.9[2]	34.6	L24	L9	L22	Routed three layers (L9, L22, and L24) short vias
–37.8[2]	26	L24	L7	L22	Routed three layers (L7, L22, and L24) short vias
–38.7[3]	26	L24	L7	L7	Routed two layers (L7 and L24) short vias
–44.3[3]	8.6	L24	L3	L3	Routed two layers (L3 and L24) short vias
–40.3[3]	26	L24	L7	L3	Routed three layers (L3, L7, and L24) short vias

Notes:

1. Not allowed.
2. OK with constraints.
3. Good.
4. This also applies to RX-RX.

TX-to-RX Crosstalk Analysis for 56 Gbps Full-density Quad Usage

Similarly, for the TX-to-RX crosstalk analysis of a triple-triple BGA pin pattern, the routing layers (via length) for the TX in the middle column are swept to understand the effects of vertical distance between TX lead-out traces and the RX via barrel to the TX-to-RX coupling.

- The routing layers for RX are constrained to L3, L5, and L7.
- The routing layer of the TX *middle* column is swept from L5, L7, L9, and L22.
- The routing layers of the TX *right* and *left* columns are kept to L22 and L24.

The following table lists the simulated power sum crosstalk for various cases. The following can be observed:

- The TX *middle* column is routed on a layer at least 18 mil (L9 – L5) below the lowest RX routing layer to fulfill the –65 dB TX-to-RX crosstalk requirement.
- While routing the TX *middle* column on L22 minimizes TX-to-RX crosstalk, it violates the –35 dB TX-to-TX crosstalk requirement due to the long via vertical parallelism.
- The attainable RX-to-RX crosstalk is –44 dB, allowing a 14 dB victim-to-aggressor insertion loss delta.

Table 3: **Simulated Power Sum Crosstalk per Via Length**

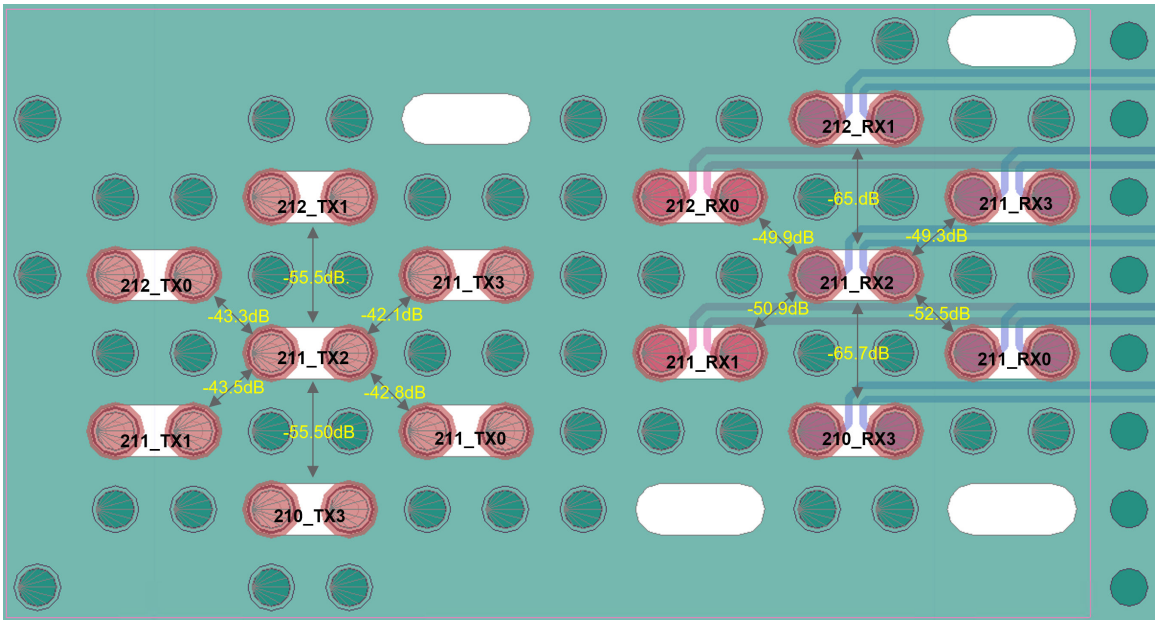
PowerSum TX-TX Xtalk (dB)	PowerSum TX-RX Xtalk (dB)	PowerSum RX-RX Xtalk (dB)	RX Routing Layers	TX Routing Layers	Comments
–28.63[1]	–68.9[3]	–43.9[2]	L3, L7	L22, L24	TX *middle* column routed on L22
–41.2[3]	–54.1[1]	–43.8[2]	L3, L7	L5, L22, L24	TX *middle* column routed on L5
–38.6[3]	–55.3[1]	–44.4[2]	L3, L5	L7, L22, L24	TX *middle* column routed on L7
–36.7[2]	–63.8[2]	–44.4[2]	L3, L5	L9, L22, L24	TX *middle* column routed on L9
–36.7[2]	–64.7[2]	–44.4[2]	L3, L5	L9, L22, L24	TX *middle* column routed on L9 with layer mis registration core L6/L7 – 4 mils

Notes:

1. Not allowed.
2. OK with constraints.
3. Good.
4. TX-TX isolation requirement is 35 dB, allowing for 5 dB TX channel insertion loss delta.
5. TX-RX isolation requirement is 65 dB, allowing for 35 dB maximum RX channel loss.
6. RX-RX isolation requirement is 45 dB, allowing for 15 dB RX insertion loss delta.

The simulated TX-to-TX and RX-to-RX crosstalk amplitudes from individual aggressors with the TX middle column routed on L9 (the fourth entry of Table 3) are shown in the following figure. It can be seen that the crosstalk from the diagonal aggressors is more severe than that from the non-diagonal aggressors. The calculated RX-to-RX power sum crosstalk is 44.4 dB, and the TX-to-TX power sum crosstalk is 36.7 dB.

Figure 17: **Simulated TX-to-TX & RX-to-RX Crosstalk with TX Middle Column Routed on L9**

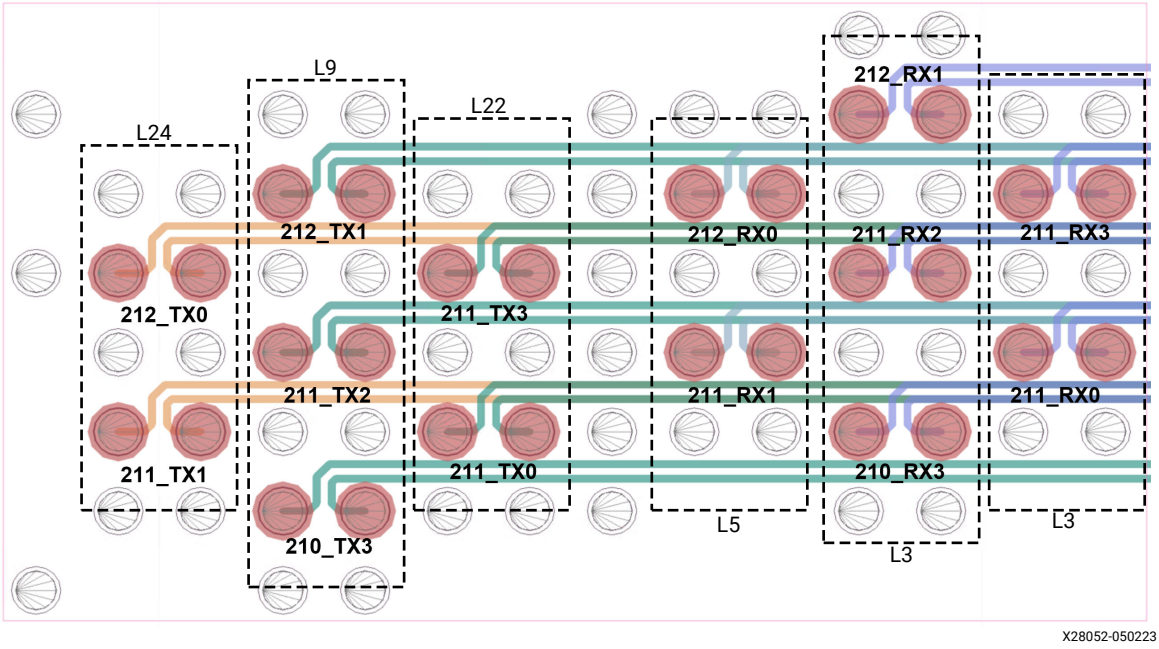


Optimal Breakout Layer Assignment for Crosstalk Mitigation

The optimal breakout layer assignment for a triple-triple BGA pin pattern identified per the sweep analysis is depicted in the following figure.

- TX port: L9 (middle column), L22, L24
- RX port: L3, L5

Figure 18: **Breakout Layer Assignment for Triple-Triple BGA Pin Pattern**

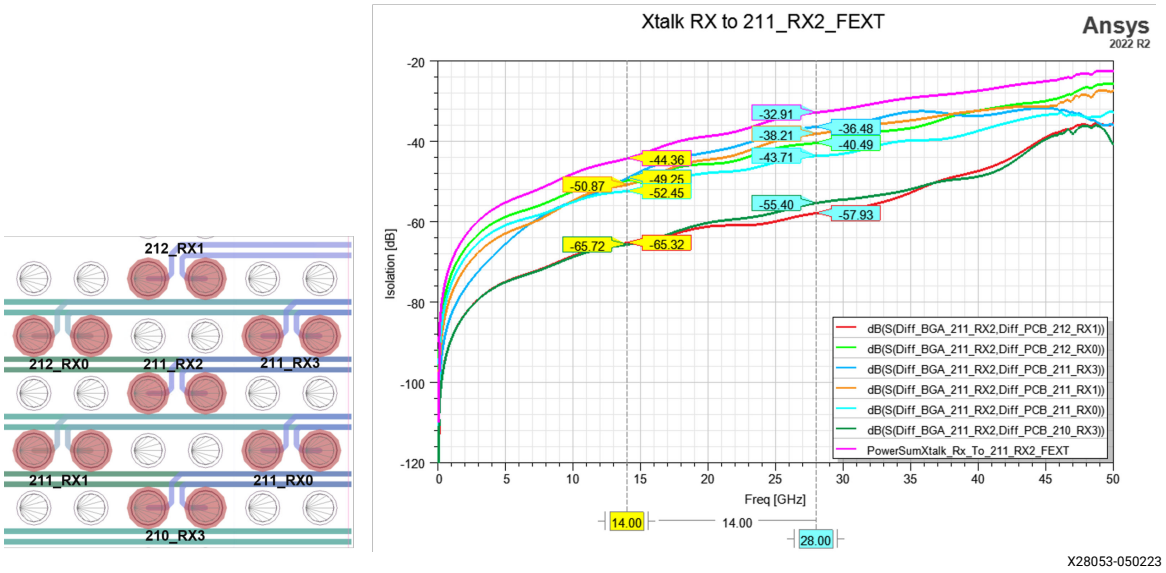


The simulated worst-case RX-to-RX crosstalk profiles, including calculated power sum crosstalk from all the aggressors based on the optimal breakout layer assignment, are shown in the following table and figure.

Table 4: **RX Routing**

Quad	Channel	Routing Layer	Via Length (mil)
210	RX3	L3	8.6
211	RX0	L3	8.6
	RX1	L5	17.3
	RX2	L3	8.6
	RX3	L3	8.6
212	RX0	L5	17.3
	RX1	L3	8.6

Figure 19: **Simulated RX-to-RX Crosstalk Based on Optimal Breakout Layer Assignment**

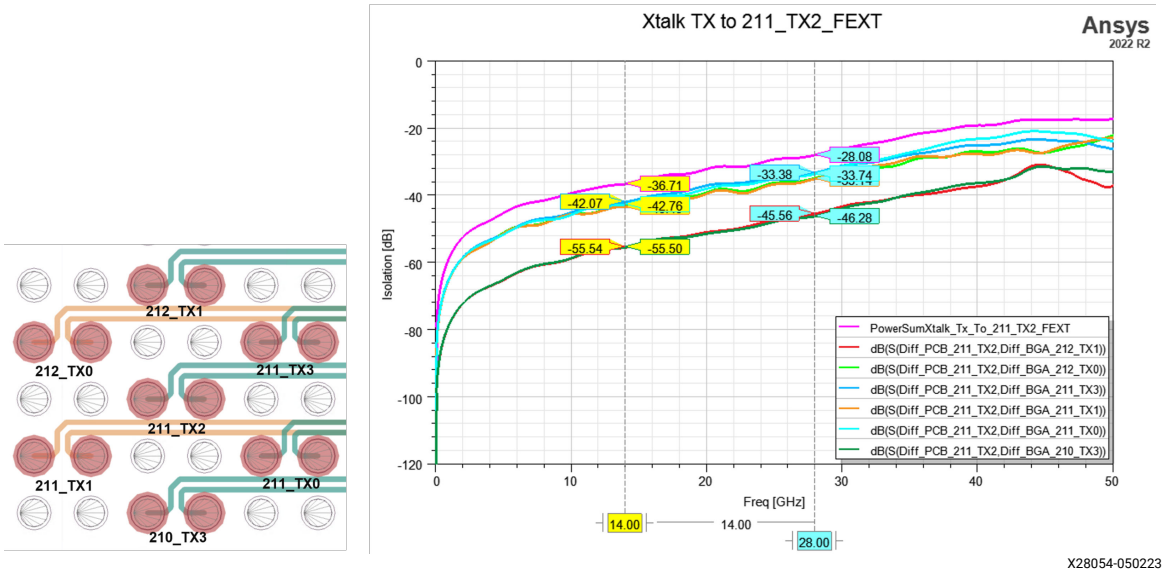


Similarly, the simulated worst-case TX-to-TX crosstalk profiles, including calculated power sum crosstalk from all the aggressors based on the optimal breakout layer assignment, are shown in the following table and figure.

Table 5: **TX Routing**

Quad	Channel	Routing Layer	Via Length (mil)
210	TX3	L9	34.6
211	TX0	L22	102.4
	TX1	L24	111.0
	TX2	L9	34.6
	TX3	L22	102.4
212	TX0	L24	111.0
	TX1	L9	34.6

Figure 20: **Simulated TX-to-TX Crosstalk Based on Optimal Breakout Layer Assignment**



***Note*:** The calculated power sum crosstalk in Figure 19 and Figure 20 includes all the adjacent aggressors, which is not the case for 112 Gbps half-density Quad.

Crosstalk Analysis for 112 Gbps Half-density (2 × GT) Quad Usage

As mentioned in TX-to-RX Crosstalk Analysis for 56 Gbps Full-density Quad Usage, crosstalk from diagonal aggressors is more severe than that from non-diagonal aggressors. Both TX-to-TX and RX-to-RX crosstalk can be limited to one diagonal aggressor by deliberately choosing the active lanes in a Quad, thereby reducing the power sum crosstalk.

The simulated TX-to-TX and RX-to-RX crosstalk amplitudes from individual aggressors for 112 Gbps PAM4 (at 28 GHz) based on the optimal breakout layer assignment are shown in the following figure and table.

Figure 21: **Simulated TX-to-TX & RX-to-RX Crosstalk Amplitudes at 28 GHz for 112 Gbps**

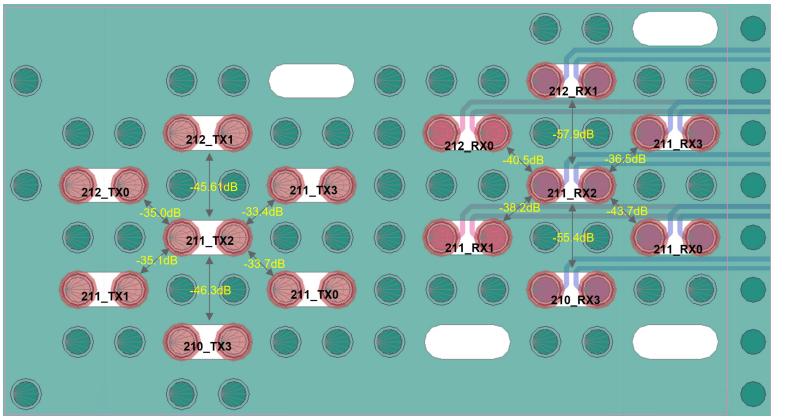


Table 6: **Simulated TX-to-TX and RX-to-RX Crosstalk Amplitudes at 28 GHz for 112 Gbps**

GM Dual Channels		Xtalk @ 112G PAM4, dB		
		RX-to-RX	TX-to-TX	TX-to-RX
211_CH0	211_CH2	–43.2	–33.7	–91.5
211_CH0	211_CH3	–44.5	–42.7	–100.9
211_CH1	211_CH2	–38.9	–35.1	–58.4
211_CH1	211_CH3	–79.5	–55.4	–65.1

C4072 Package PCB Breakout Design Guidance

The recommendations for the C4072 package PCB breakout are summarized as follows.

- TX-to-RX isolation must be carefully considered, especially for LR applications
- RX-to-RX isolation for large IL variations must be carefully considered
- Route TX on lower layers rather than RX to avoid trace-to-via coupling
- Provide ~18 mil separation between RX and TX routing layers
- Place GND vias outside BGA pins to improve RX-to-RX isolation

For a 56 Gbps full-density Quad usage, recommendations are as follows:

- TX-to-TX crosstalk
  - Worst-case TX victim: Four diagonal aggressors (plus two non-diagonal aggressors separated by a pair of GND balls)
  - *Middle* column of TX pins routed with via length less than 45 mil
  - Victims with fewer aggressors can have longer vias
- RX-to-RX crosstalk
  - Worst-case RX victim: Four diagonal aggressors (plus two non-diagonal aggressors separated by a pair of GND balls)
  - Projected power sum crosstalk at < 14 GHz = –44 dB
  - Recommended restriction: Insertion loss delta between RX channels: < 14 dB
- TX-to-RX crosstalk
  - For LR RX with 35 dB insertion loss, requirement is 65 dB isolation
  - TX routing layer must be at least 18 mil below lowest RX routing layer

Reference Design

Download the reference design files for this application note from the Adaptive SoC Transceiver IBIS-AMI Model Secure website.

Reference Design Matrix

The following checklist indicates the procedures used for the provided reference design.

Table 7: **Reference Design Matrix**

Parameter	Description
General	
Developer name	AMD
Target devices	Versal Premium, Prime, and HBM series
Source code provided?	Y
Source code format (if provided)	IBIS-AMI model
Design uses code or IP from existing reference design, application note, third party or AMD Vivado™ software? If yes, list.	N
Simulation	
Functional simulation performed	N
Timing simulation performed?	N
Test bench provided for functional and timing simulation?	N
Test bench format	N/A
Simulator software and version	Ansys Electronics Desktop, Keysight ADS
SPICE/IBIS simulations	Y
Implementation	
Implementation software tool(s) and version	N/A
Static timing analysis performed?	N
Hardware Verification	
Hardware verified?	Y
Platform used for verification	VPK180

Conclusion

This application note reviews the 112 Gbps PAM4 design challenges and the various impairments on the PCB channel. It specifies the Versal device GTM transceiver PCB channel design requirements in terms of channel insertion loss, return loss, crosstalk, and intra-pair skew. The application note also demonstrates good practices for minimizing and mitigating various impairments and fulfilling the corresponding channel design requirements.

References

These documents provide supplemental material useful with this application note:

1. Yohan Frans, IEEE Education Session, Overview of ADC-based Wireline Transceiver, CICC 2019
2. Geoff Zhang, et al, *A Tutorial on PAM4 Signaling for 56G Serial Link Applications*, DesignCon 2017

3. OIF Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements: OIF-CEI-04.0
4. IEEE standards for Ethernet: IEEE Std 802.3bs-2017, IEEE Std 8023cd-2018, and IEEE Std 802.3ck-2022
5. *Versal Adaptive SoC GTM Transceivers Architecture Manual* (AM017)
6. *Versal Prime Series Data Sheet: DC and AC Switching Characteristics* (DS956)
7. *Versal Premium Series Data Sheet: DC and AC Switching Characteristics* (DS959)
8. *Versal HBM Series Data Sheet: DC and AC Switching Characteristics* (DS960)
9. Eben Kunz, et al, *Sources and Compensation of Skew in Single-Ended and Differential Interconnects*, DesignCon 2014
10. Eric Bogatin, et al, *New Characterization Technique for Glass-Weave Skew*, DesignCon 2016/2017
11. Scott McMorrow, et al, *The Impact of PCB Laminate Weave on the Electrical Performance of Differential Signaling at Multi-Gigabit Data Rates*, DesignCon, 2005
12. Jeff Loyer, et al, *Fiber Weave Effect: Practical impact Analysis and Mitigation Strategies*, DesignCon 2007
13. *Versal Adaptive SoC Packaging and Pinouts Architecture Manual* (AM013)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
05/23/2023 Version 1.0	
Initial release.	N/A

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