Zynq-7000 SoCs or 7 Series FPGAs Isolation Design Flow Lab (Vivado Design Suite)

XAPP1256 (v1.2) October 20, 2023

Summary

This lab application note describes the creation and implementation of a single chip cryptography (SCC) system using redundant Keccak hash modules with compare logic. Complete step-by-step instructions are given for the entire process, explaining the use of the Isolation Design Flow (IDF). This document explains how to implement isolated functions in a single AMD Zynq™ 7000 SoC device for the example SCC solution. Even though this application note explains how to implement a design using the IDF for a Zynq 7000 device, the same process can be used to implement an IDF design using any 7 series FPGA device.

With this application note, designers can develop a fail-safe single chip solution using the IDF that meets fail-safe and physical security requirements for an example high-assurance application.

This application note is similar to the application note 7 series Isolation Design Flow Lab Using ISE Design Suite 14.4 (XAPP1085) with the primary difference being this document is specific to using the AMD Vivado™ Design Suite for Zynq 7000 SoC devices, whereas *7 Series Isolation Design Flow Lab Using ISE Design Suite 14.4* (XAPP1085) is specific to using the AMD ISE® Design Suite for developing IDF designs for 7 series FPGA devices. The rules for IDF defined in this application note do not differ from those defined in XAPP1085, but the methodology for implementation using Vivado tools does.

This application note is accessible from the Isolation Design Flow website.

Download the Reference Design Files for this application note from the Xilinx website. For additional information about the design files, see Reference Design Files.

Introduction

The Isolation Design Flow is the software methodology that allows for SCC implementations or any other application requiring the module have both physical and logical isolation. This methodology is backed by significant schematic analysis and software verification—Vivado Isolation Verifier (VIV)—to ensure elimination of single points of failure. SCC is one specific application of IDF allowing the implementation of a multichip cryptography system in a single FPGA or SoC.

Note: Procedure will work with Vivado versions 2018.3 and later.

Lab Design Overview

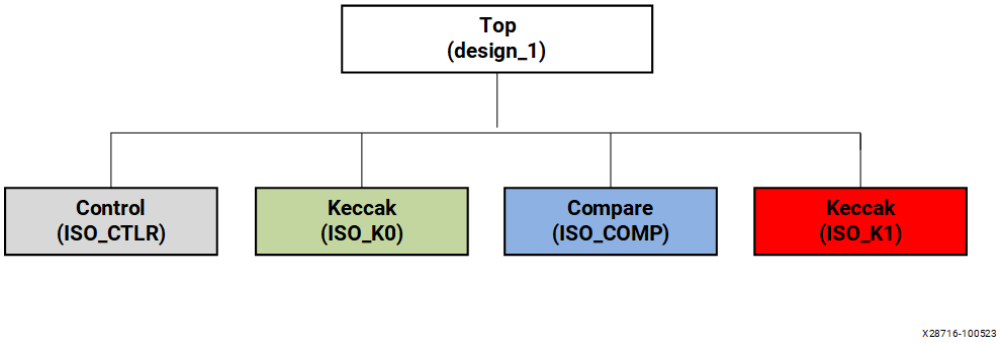
The 7 series and Zynq 7000 IDF rules are outlined in Isolation Design Flow for 7 series FPGAs or Zynq 7000 SoCs (Vivado Tools) (XAPP1222). Though the rules for IDF do not differ between ISE and Vivado, the methodology for implementation using Vivado tools does differ.

This lab gives details on how functions are to be isolated, specific differences between a normal partition flow and an IDF partition flow, information on IDF-specific hardware description language (HDL) code mnemonics, and trusted routing rules.

To illustrate the IDF and its capabilities, this design implements isolated, redundant Keccak hash modules with a compare block. The following figure is a hierarchical diagram of the various VHDL sub-blocks used in the implementation of this design.

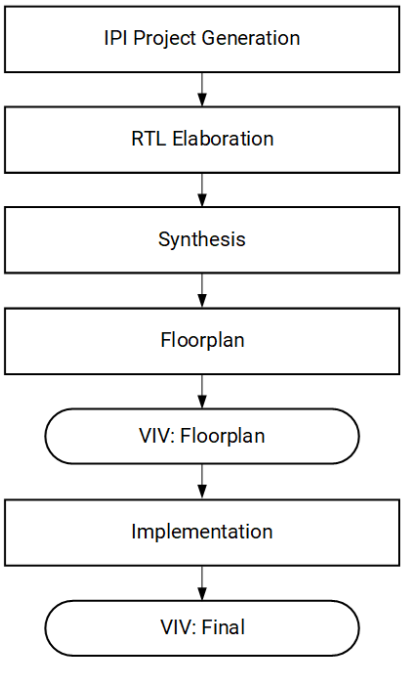
IMPORTANT! *Use Vivado Integrated Design Environment (IDE) 2018.3 or later for this lab.*

Figure 1: **Design Hierarchy Block Diagram**



The following figure shows the flow used during the course of this lab. The fundamental goal is to give you an idea of what the methodology looks like in Vivado tools and how tools such as Vivado IP integrator can be of significant help (see *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994).

Figure 2: **Vivado IDF Lab Flow Using IP Integrator as the Primary Source Generator**

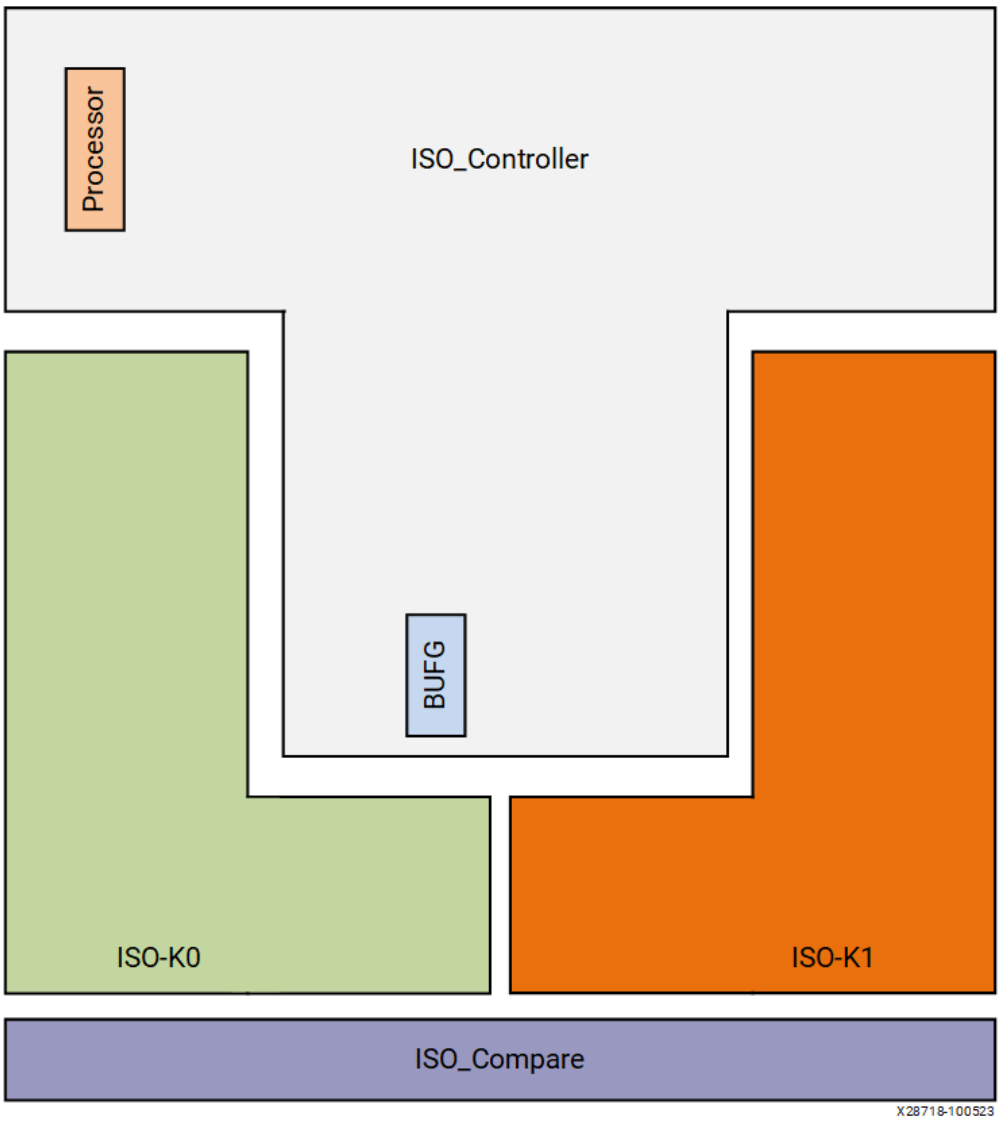


The following figure shows the floorplan for the lab design as implemented in an xc7z020clg484-1 device. It consists of four area groups. The first is an area group that contains the PS7 site (Arm® Dual Core A9 Processing System) and some additional space to route as needed, such as Advanced eXtensible Interface (AXI) signals. The other three represent a typical redundant system with compare module whose clocks and resets come from the processor.

IMPORTANT! *When putting the PS7 in an area group, at the very minimum, create a fence on the full right side of the PS7 block and include the first CLB tile on the lower right corner under the PS7 block. See Isolation Design Flow for Xilinx 7 Series FPGAs or Zynq-7000 SoCs (Vivado Tools) (XAPP1222), PS Fence Tile section, for more details.*

Signals from the PS7 can only get to the FPGA fabric on the right side of the PS7 site. If you need to communicate to an area group below the PS7, you need to have added some of the fabric on the right and bottom to allow communication to and from the PS7.

Figure 3: **Die View: IDF Lab Floorplan in an xc7z020clg484-1 Device**



Install Reference Design Files into Target Directories

These steps describe the process for installing the reference design files:

***Note*:** For this lab, it is important that the design files are in a known location, in this case, `C:\xilinx_design`.

1. Extract the `xapp1256-idf-for-zynq-vivado.zip` file to your home drive letter (that is, `C:`).
2. The project files are placed in the `C:\xilinx_design\sources\` directory.
   - `xilinx_design`
     - `sources`
       - `ip`
       - `viv`

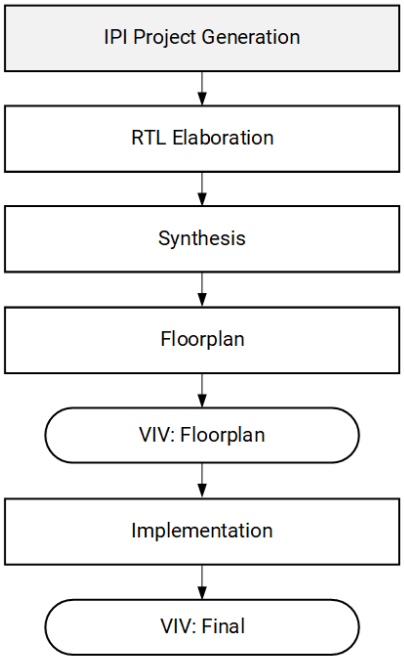
- `xdc`

When the ZIP file is extracted, a directory called `xilinx_design` holds the lab project design files. The directory structure shown above applies to that project.

Creating a Vivado IP Integrator Project

This section describes the steps that take you through a bottom-up synthesis flow, using the Vivado Design Suite, which is the flow used for IDF designs to maintain isolation. Vivado allows you either to create designs manually or import register-transfer level (RTL) source code directly into the project so the project can be done using the Vivado tool. Refer to the Lab Flow Progression flow chart in the following figure.

Figure 4: **Lab Flow Progression – Vivado IP Integrator Project**



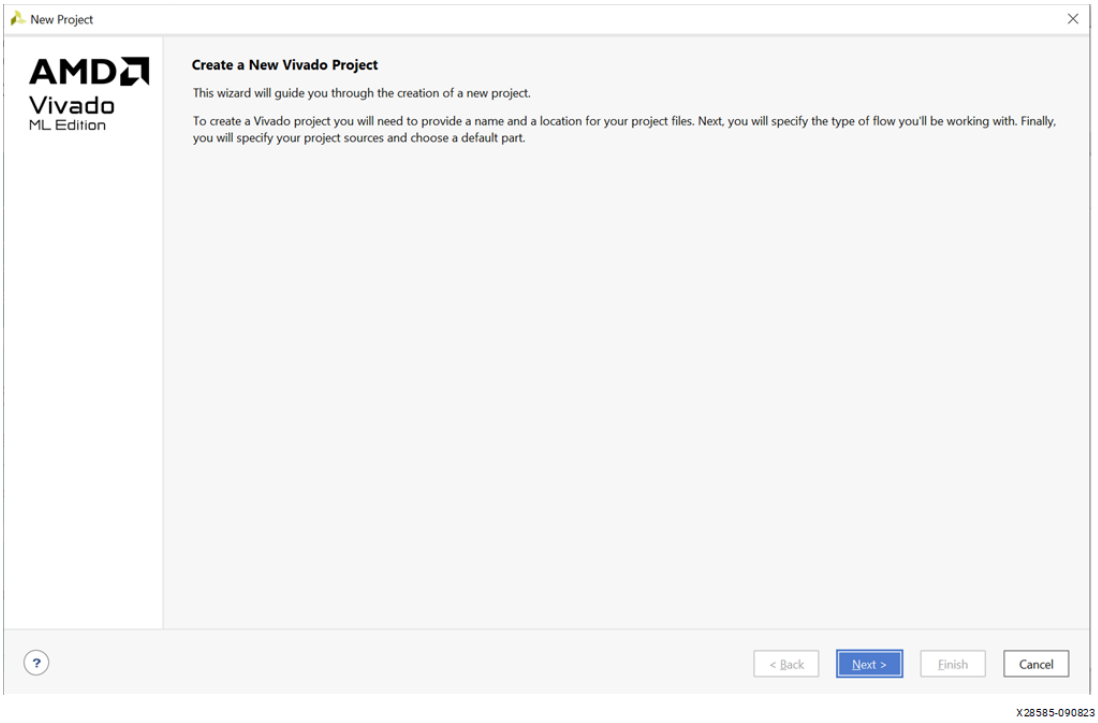
Project Entry in Vivado

Vivado Project Creation

The Vivado tool works with any standard RTL source files. The regular guidelines are followed to generate a new project and import the RTL source files into the Vivado tool to create a floorplan for the design.

1. Set up a new Vivado project: From the Quick Start menu, click Create New Project, and wait for the New Project - Create a New Vivado Project window to pop up (see the following figure). Select **Next**.

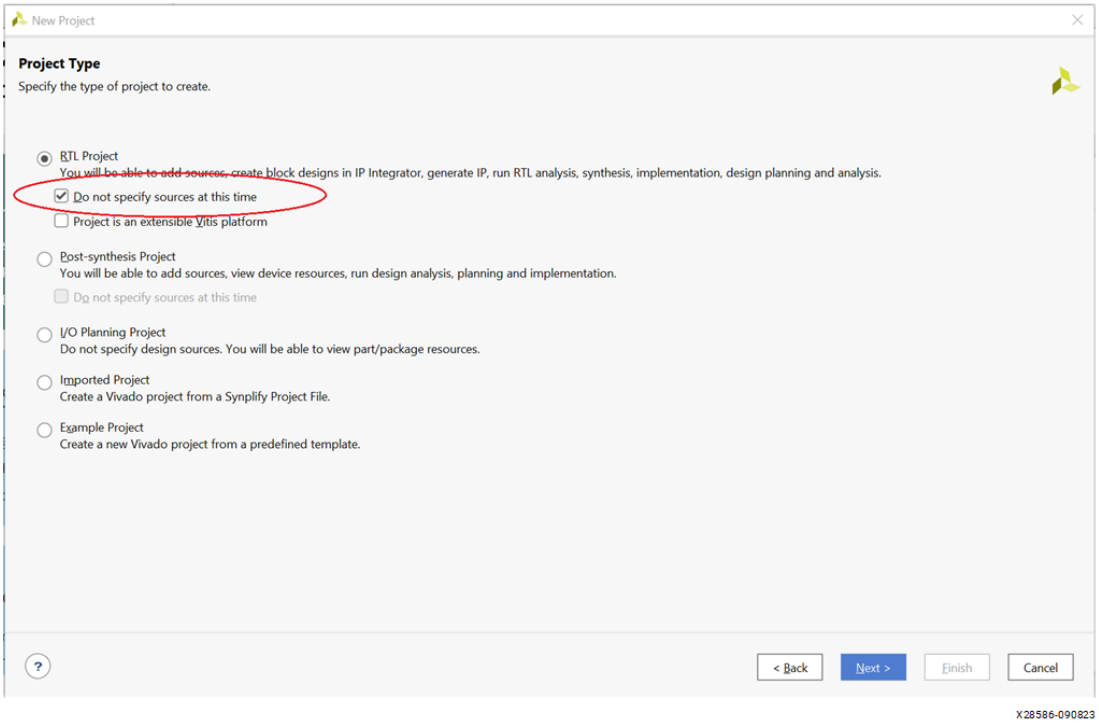
Figure 5: **Vivado New Project > Project Name Window**



2. In the *New Project - Project Name* window enter:
   - **Project name:** For this lab, the *idfLab* project name is used.
   - **Project location:** `C:/xilinx_design`. This directory does not exist and is created by the Vivado tool.

     ***Note*:** The Vivado tool automatically changes the Windows directory path separator from \ (back slash) to / (forward slash).
   - Select Create project sub-directory.
3. Click **Next**.
4. Select RTL Project and check the Do not specify sources at this time box (see the following figure).

Figure 6: **Vivado New Project - Project Type Window**



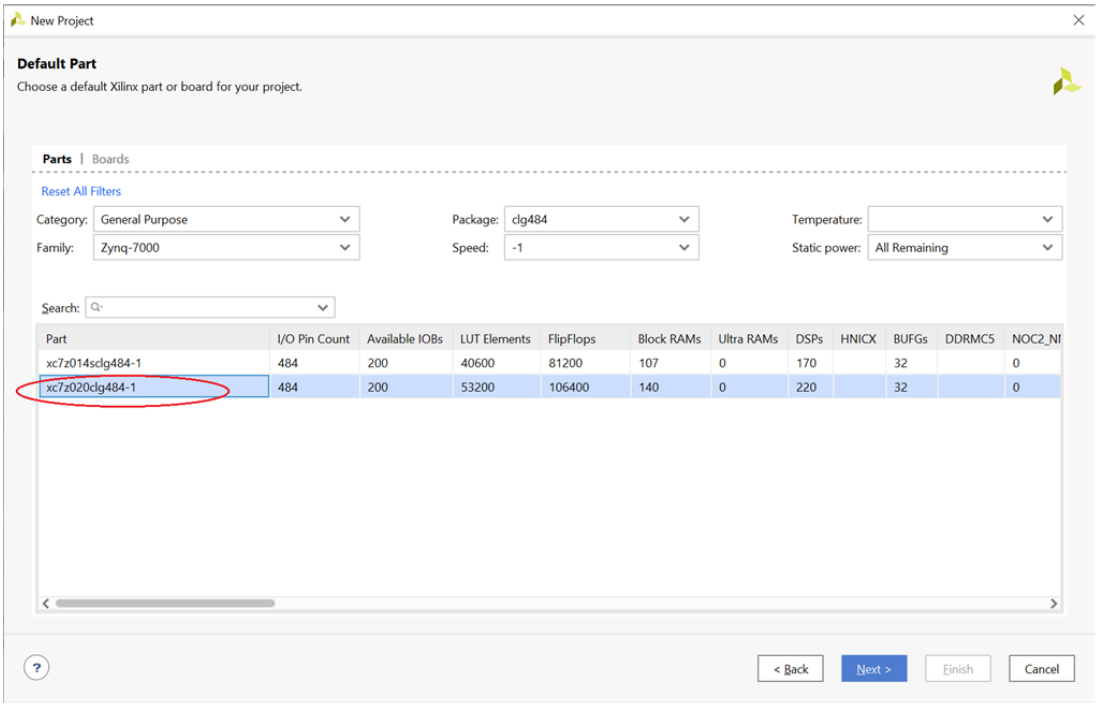
***Note*:** RTL sources are added later.

5. Click **Next**.
6. In the Default Part window, select the appropriate product filters for this lab as listed here and shown in Figure 7.

Product category	General Purpose
Family	Zynq 7000
Sub-Family	Zynq 7000
Package	clg484
Speed grade	-1
Temp grade	C
Si Revision	All Remaining

7. Select the xc7z020clg484-1 device.
8. Click **Next** and **Finish**.

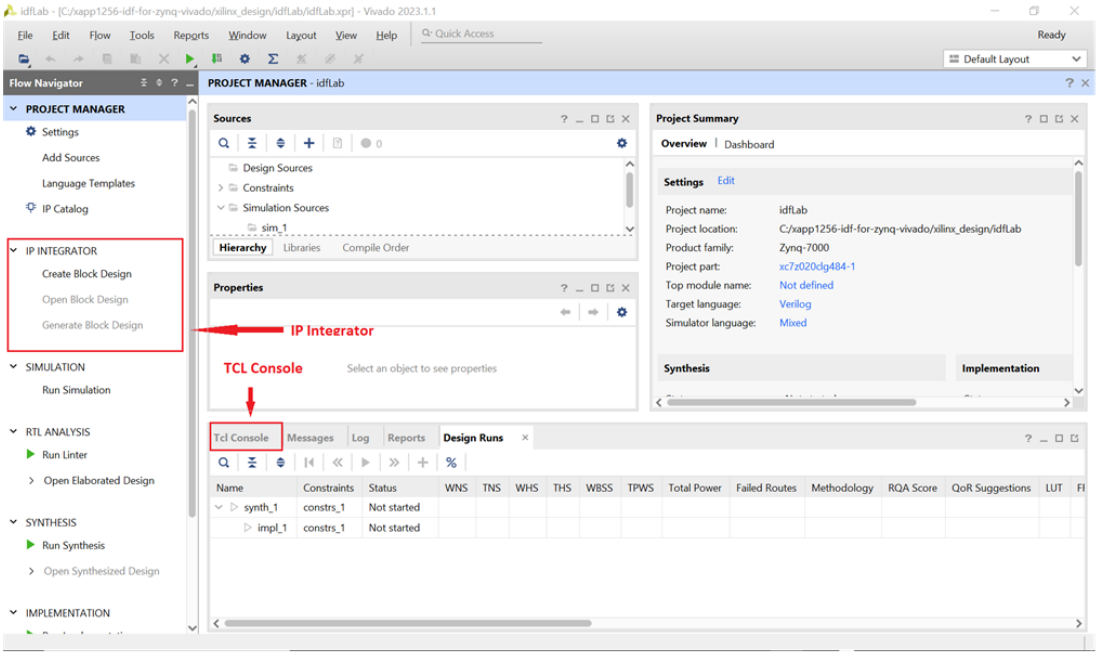
Figure 7: **Vivado New Project – Default Part Window**



X28587-090823

9. The Vivado project now is created. The following figure shows the Project Manager window for the idfLab project.

Figure 8: **Plan Ahead Project Manager View**



X28588-090823

Launch the Vivado IDE

Launch the Vivado tool from the installed location.

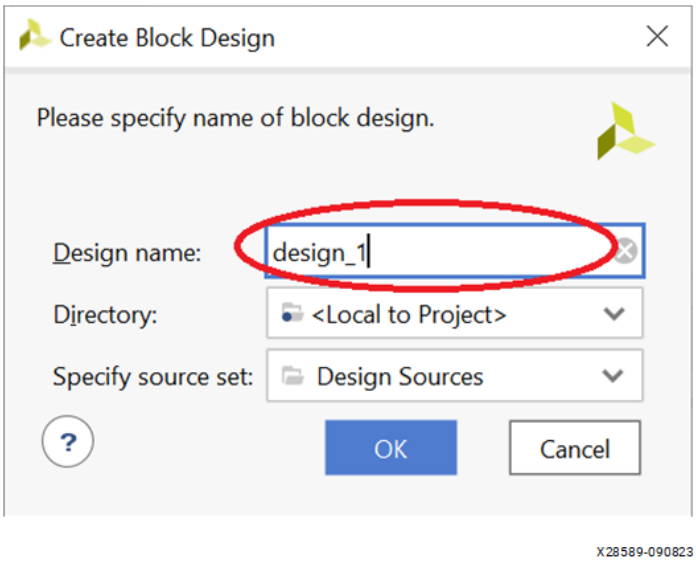
Building the IP Integrator Project

In this lab, you build a system using existing IP. Because some of this IP is custom, it is necessary to tell Vivado IP integrator where the custom IP is located so it can import that IP into the IP library.

1. Select the Tcl Console tab at the bottom left of the Vivado GUI (see the previous figure).
   a. Type `cd c:/xilinx_design` on the Tcl console line. This is important because future commands in this lab rely on this being the active directory.
   b. Type `set_property ip_repo_paths ./sources/ip [current_fileset]` on the Tcl console line. This command sets the path to point to the location of the custom IP.
   c. Type `update_ip_catalog` on the Tcl console line. This command refreshes the IP repositories with the user IP repository

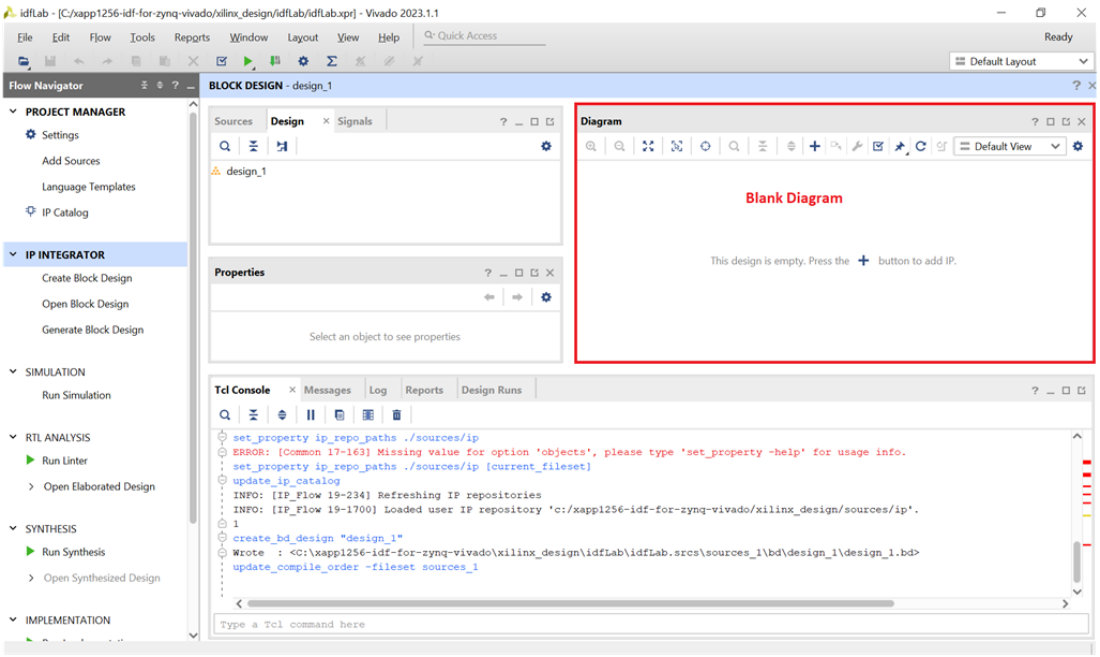
      ***Note*:** These steps can also be accomplished in the GUI by going to IP settings in the Project Settings found in the Project Manager section on the top left of the Vivado GUI.
2. Create an IP integrator block design in the IP integrator tool by navigating to the Project Manager pane on the left and select IP Integrator > Create Block Design (see the previous figure).
3. Keep the default design name *design_1* and select **OK** (see the following figure).

Figure 9: **Create Block Design > Set Design Name**



4. You should see a blank diagram, as shown in the following figure.

Figure 10: **IP Integrator Block Diagram**

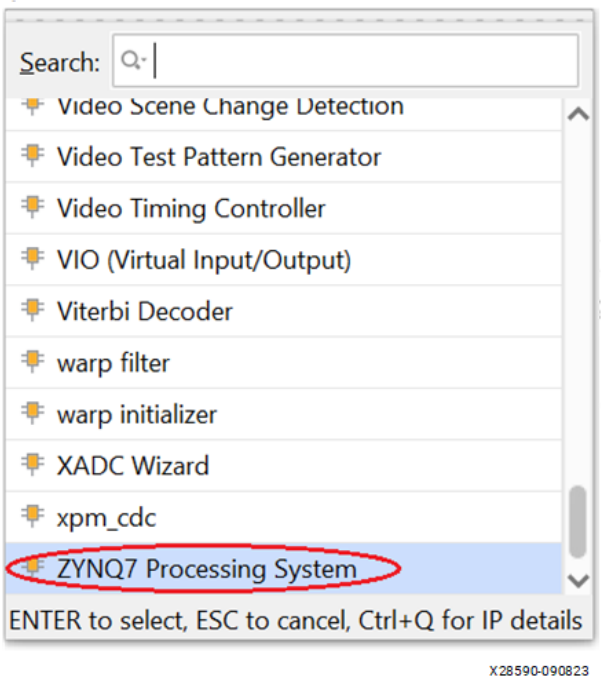


Creating an IP Integrator Block Design

The purpose of using IP integrator in this lab is to demonstrate the ease with which a hierarchy can be added to a flat design (one not originally intended to be implemented using IDF). Additionally, it turns creating a redundant design into a copy/paste operation.

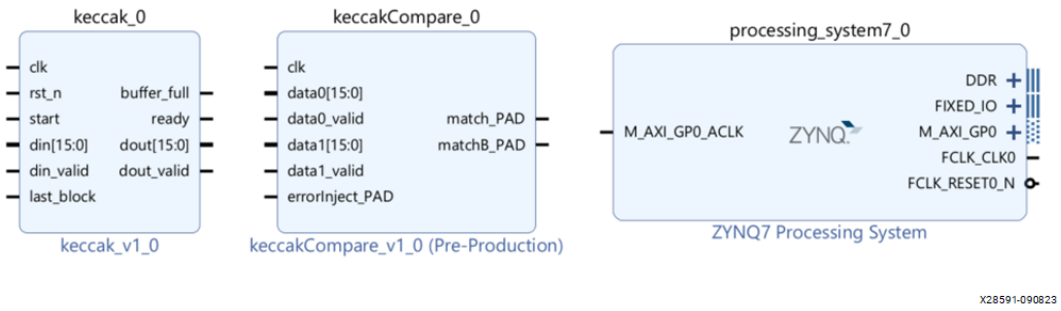
1. Right-click the Diagram canvas and select Add IP.
2. Scroll to the ZYNQ7 Processing System IP, select it, and press Enter (see the following two figures).

Figure 11: **Add IP > ZYNQ7 Processing System**



3. Repeat Step 1 for the keccakCompare_v1_0 IP (see the following figure).
4. Repeat Step 1 for the keccak_v1_0 IP (see the following figure).

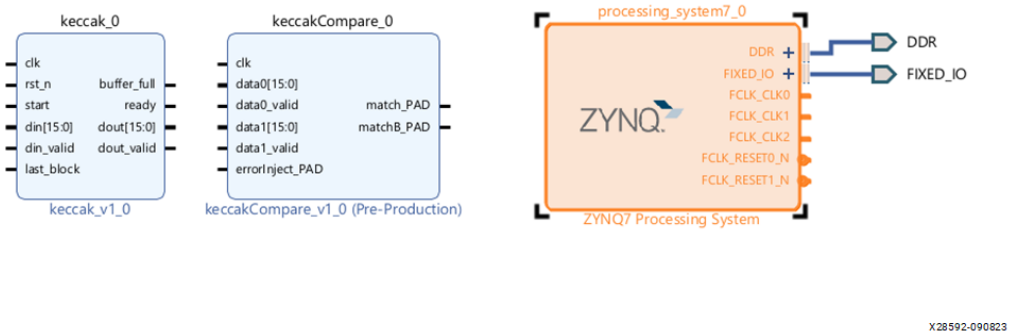
Figure 12: **IP Integrator Canvas after IP Selection**



Now that all the necessary blocks have been added (see the previous figure), it is time to start constructing the design. First, the processor is configured. In this lab, the processor's sole function is to source the clocks and resets to your design.

5. **Save** the design.
6. Double-click the processing_system7_0 IP instance (to re-customize the IP).
   a. Under PS-PL Configuration, expand the AXI Non Secure Enablement > GP Master AXI Interface item and deselect the M AXI GP0 interface.
   b. In the Search box at the top, enter reset and select FCLK_RESET0_N (default) and FCLK_RESET1_N.
   c. Under Clock Configuration, expand the PL Fabric Clocks item and select FCLK_CLK0 (default), FCLK_CLK1, and FCLK_CLK2. Keep their default parameters for these clocks.
   d. Select **OK**.
   e. With the processor block still selected, select Run Block Automation at the top of the IP integrator canvas (navigating the mouse to select processing_system7_0/).
   f. Click **OK** to run block automation. The canvas should look like the following figure.

Figure 13: **IP Integrator Canvas after Running Block Automation**



7. Wire up the first instance of the **Keccak** hash block.
   a. Point at dout[15:0] of the keccak_0 instance until the mouse arrow turns into a pencil. Click and drag the wire to the data0[15:0] port of the keccakCompare_0 instance.
   b. Repeat *Step a* connecting dout_valid to data0_valid.
   c. Right-click buffer_full and select make external.
   d. Repeat *Step c* for ready.
   e. Repeat *Step c* for start.
   f. Repeat *Step c* for din[15:0].
   g. Repeat *Step c* for din_valid.
   h. Repeat *Step c* for last_block.
8. Wire up the second instance of the Keccak hash block. In this case, you must first create it.

a. Right-click keccak_0 and select Copy. Select elsewhere on the canvas, right-click, and select Paste.

b. Point at dout[15:0] from the keccak_1 instance until the mouse arrow turns into a pencil. Click and drag the wire to the data1[15:0] port of the keccakCompare_0 instance.

c. Repeat *Step b* connecting dout_valid to data1_valid.

d. Right-click buffer_full and select make external.

e. Repeat *Step d* for ready.

f. Repeat *Step d* for start.

g. Repeat *Step d* for din[15:0].

h. Repeat *Step d* for din_valid.

i. Repeat *Step d* for last_block.

9. Wire up the compare block.

   a. Right-click match_PAD and select make external.

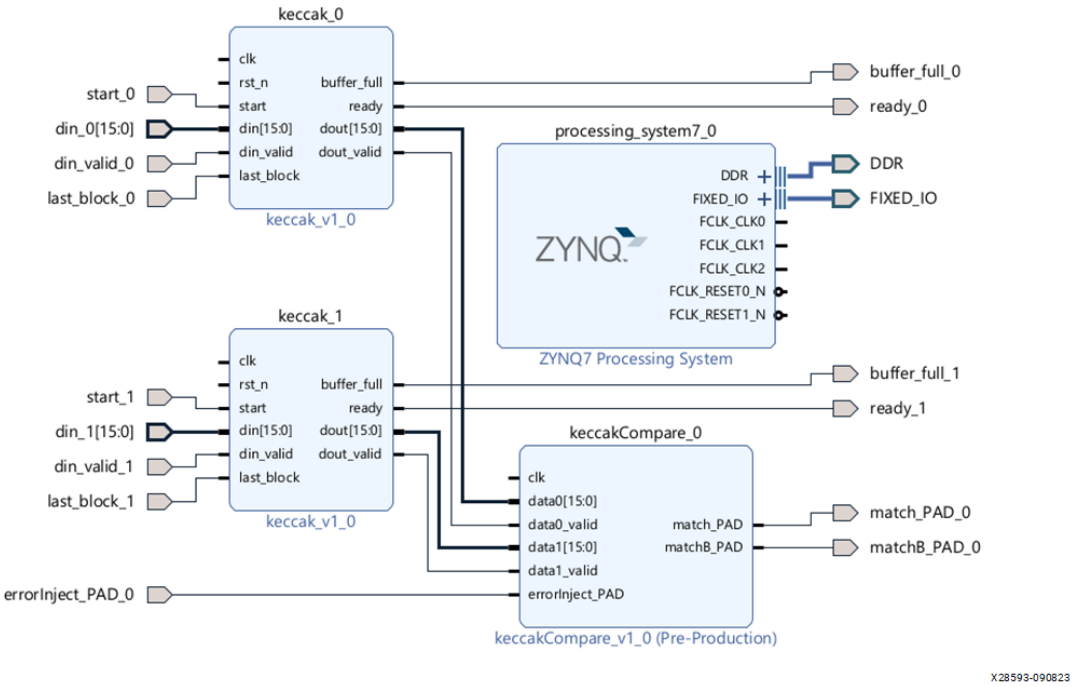
   b. Repeat *Step a* with matchB_PAD.

   c. Repeat *Step a* with errorInject_PAD.

10. **Save** the design.

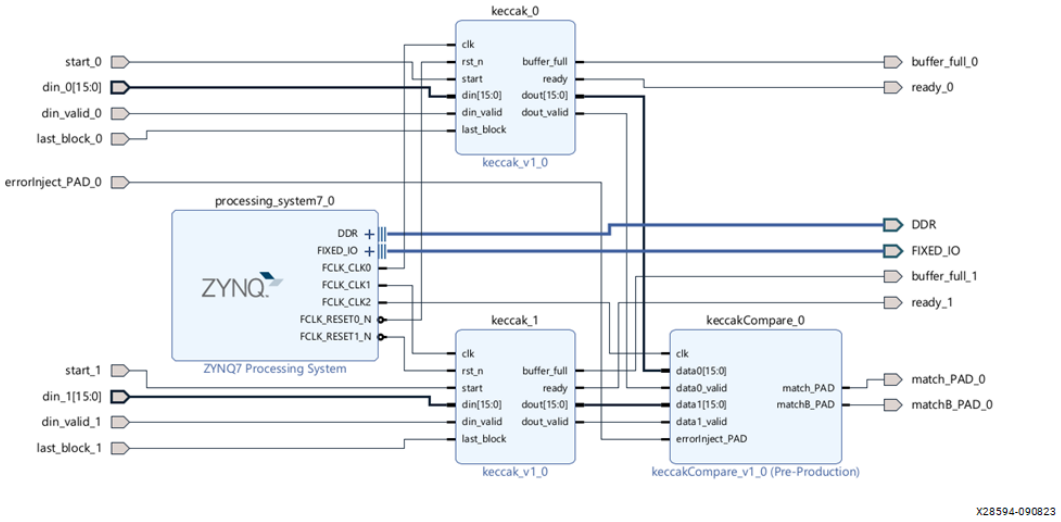
11. Right-click an empty space in the canvas and select Regenerate Layout. The IP integrator canvas should look like the following figure:

Figure 14: **IP Integrator Canvas after Initial Connections**



12. Connect the clocks and resets.
    a. Draw a wire from FCLK_CLK0 of the processing_system7_0 IP to the *clk* input of the keccak_0 instance.
    b. Draw a wire from FCLK_RESET0_N of the processing_system7_0 IP to the *rst_n* input of the keccak_0 instance.
    c. Repeat *Step a* and *Step b* for the keccak_1 instance using FCLK_CLK1 and FCLK_RESET1_N, respectively.
    d. Draw a wire from FCLK_CLK2 of the processing_system7_0 IP to the *clk* input of the keccakCompare_0 instance.
    e. Click **Save**.
    f. Select Regenerate Layout. This is for ease of viewing. Your canvas should now look like the following figure.

Figure 15: **IP Integrator Canvas after Final Connections**



13. Each of the four blocks in the previous figure are modules that need to be isolated.

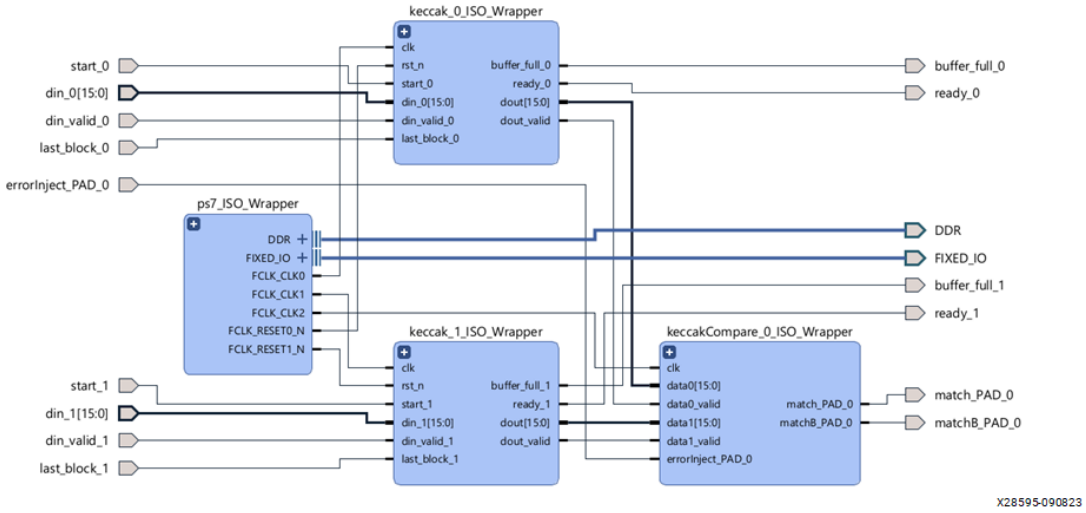
> **IMPORTANT!** *IP integrator introduces some design complexities by automatically adding DONT_TOUCH properties on every design block of an IP integrator design. This conflicts with IDF where multi-regional nets are concerned. To split multi-regional nets to meet IDF rules, the tools must modify the design by adding LUT buffers. However, DON'T_TOUCH prevents any modification by the tools. Much of this complexity can be minimized by adding a wrapper around modules intended for isolation. Ultimately, it is the wrapper that is marked as isolated. Such wrappers are not required for custom HDL designs not implemented using IP integrator.*

14. Right-click keccakCompare_0 and select Create Hierarchy ...
    a. Name it keccakCompare_0_ISO_Wrapper.
    b. Make sure the check box to add the selected instance is selected and select **OK**.
15. Repeat Step 14 for keccak_0 naming it keccak_0_ISO_Wrapper.
16. Repeat Step 14 for keccak_1 naming it keccak_1_ISO_Wrapper.
17. Repeat Step 14 for processing_system7_0 naming it ps7_ISO_Wrapper.

***Note*:** A critical message pops up noting that it is necessary to associate ELF files. Select **OK**. There are no such files in this project and they would get regenerated anyway in future steps.

18. Verify all connections are valid by right-clicking on the blank canvas and selecting Validate Design. Select **OK** to continue.
19. **Save** the design.
20. Select Regenerate Layout. This is for ease of viewing. Your canvas should now look like the following figure.

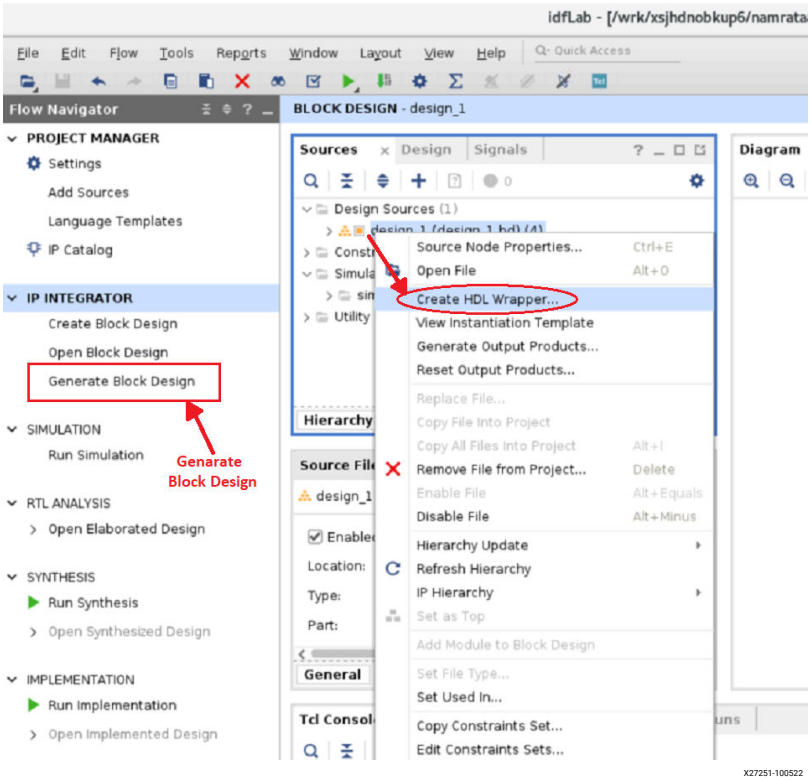
Figure 16: **Final IP Integrator Canvas**



21. Generate all necessary output products for the block design you just created.
    a. In the Sources tab, right-click design_1 and select Create HDL Wrapper as shown in the following figure. On the pop-up window, select Let Vivado manage the wrapper and auto-update and select **OK**.
    b. Under the IP Integrator menu on the left, select Generate Block Design as shown in the following figure. Select Generate on the pop-up window. Select **OK** when the process completes.

       ***Note*:** Recall the critical warning with respect to ELF files. This warning is addressed in this step.
22. The design is now ready for the RTL elaboration phase. **Save** the design.

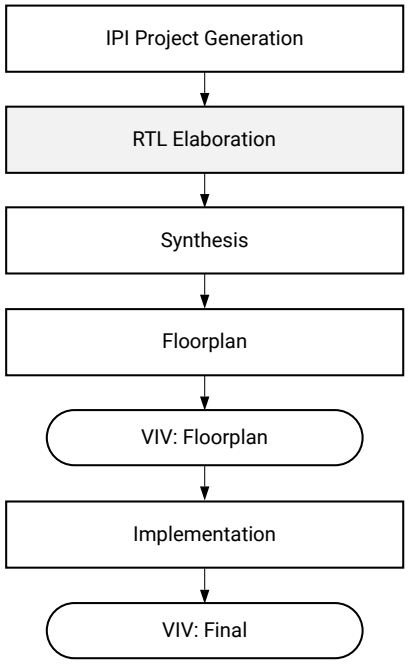
Figure 17: **Create HDL Wrapper/Generate Block Design**



Design Elaboration

Register-transfer level (RTL) design elaboration is a small step in this lab. Its primary function is to debug the HDL code of the design as shown in the following figure.

Figure 18: **Lab Flow Progression - RTL Elaboration**

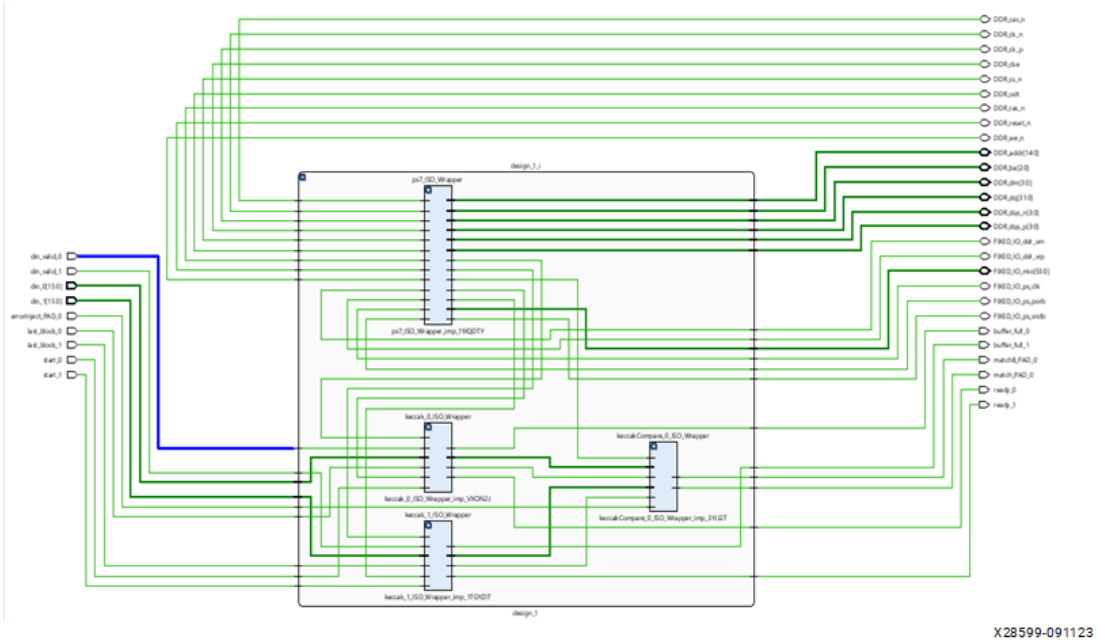


Open the Elaborated Design

Just under the IP Integrator section is the Simulation section and then the RTL Analysis section.

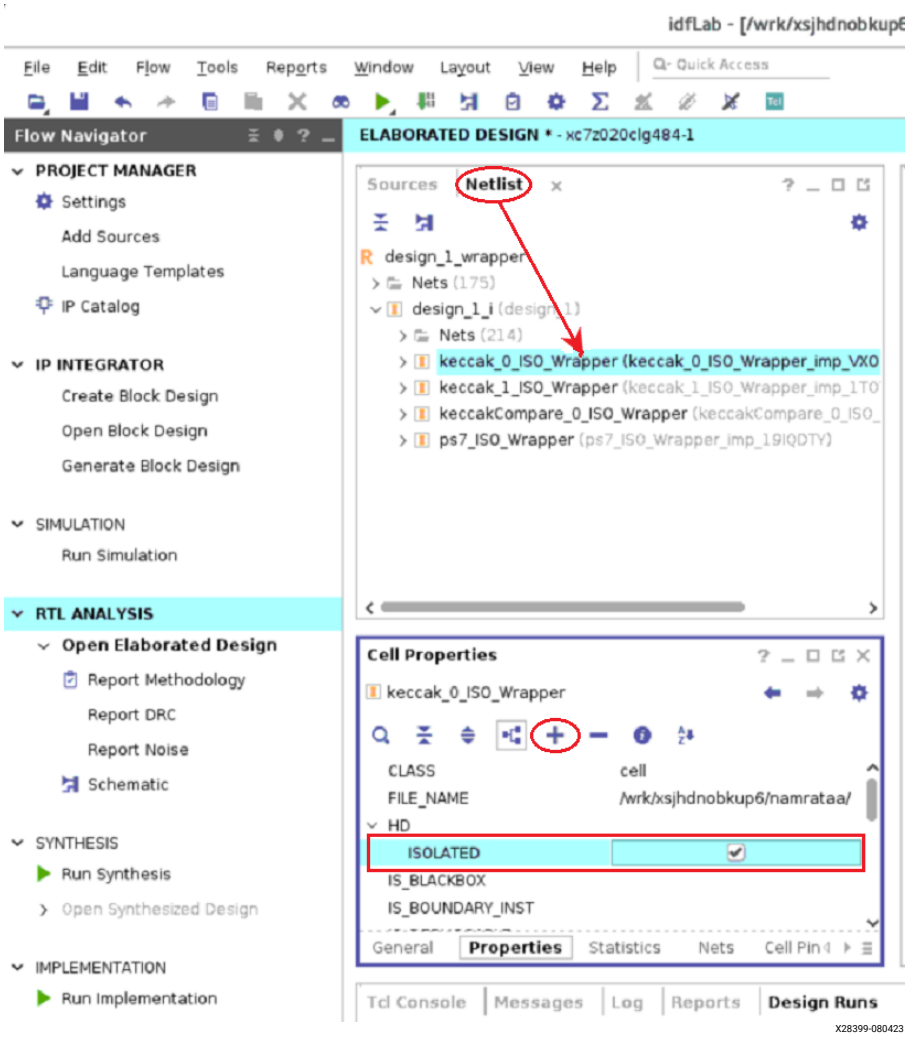
1. Click the Open Elaborated Design menu item. This launches the process. When complete, a large block diagram labeled design_1_i will appear. This is the default name generated by IP integrator when the HDL wrapper was added.
2. Navigate to your design by clicking **+** at the top left of any block to open hierarchies. The following figure shows an example of one hierarchy opened.

Figure 19: **RTL Schematic (expanded)**



3. Add some attributes to tell the tools which modules are going to be isolated using IDF. This is done with the `HD.ISOLATED` attribute. This attribute not only evokes the IDF routing rules, but also protects redundant modules from undesired optimization. Synthesis optimization cannot happen across an `HD.ISOLATED` boundary. It can happen within one, but that is typically desired.
4. Expand the design_1_i instance in the Netlist tab so each of the modules created in IP integrator are visible as shown in the following figure.
5. Select keccak_0_ISO_Wrapper.
   a. Right-click and select Cell Properties (if this window is not already visible).
   b. Select the Properties tab in the *Cell Properties* window.
   c. Click the green **+** and add the attribute *HD.ISOLATED* from the Add Properties pop-up window.
   d. Expand the newly added attribute and check the unchecked check box as shown in the following figure.

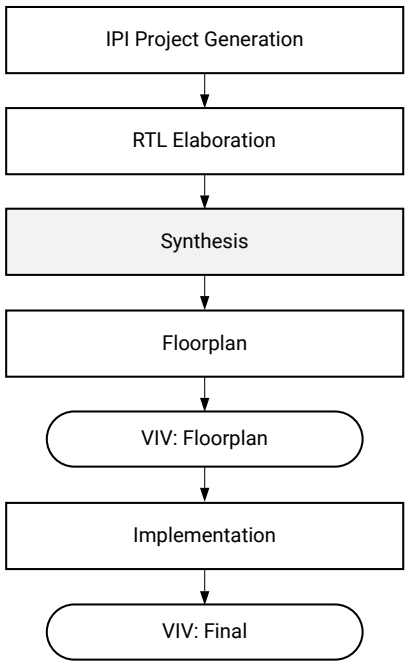
Figure 20: **Setting HD.ISOLATED Attribute**



6. Repeat Step 5 for keccak_1_ISO_Wrapper.
7. Repeat Step 5 for keccakCompare_0_ISO_Wrapper.
8. . Repeat Step 5 for ps7_ISO_Wrapper.
9. Save the design and enter Top when requested, to enter the file name of the Xilinx design constraints (XDC) file
10. Select **OK**.

Design Synthesis

Figure 21: **Lab Flow Progression - Synthesis**



Synthesis Process

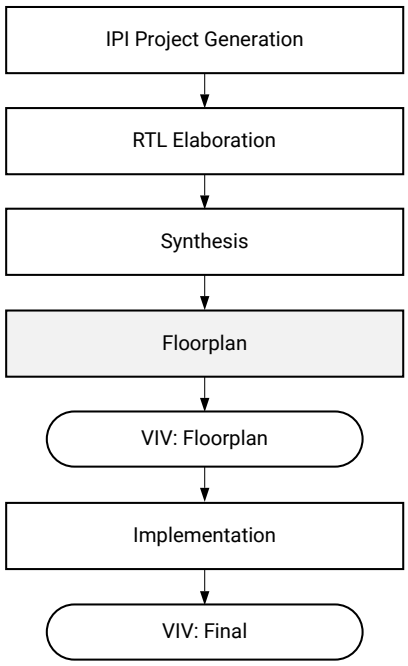
This section describes the synthesis process. In this lab, though time consuming, synthesis is not a significant part of the process. This is because all the IP was created earlier and you are only assembling the blocks. If done correctly, the synthesis schematic should look the same as the RTL schematic.

Launch Synthesis

1. Under the Synthesis menu on the left of the Vivado GUI, select Run Synthesis. If prompted, save the design.
2. When complete, change the check box to Open Synthesized Design and click **OK**.
3. If asked to close the Elaborated Design before opening the Synthesized Design, do so by selecting **Yes**. This is good practice because memory might be limited.

Floorplanning the System

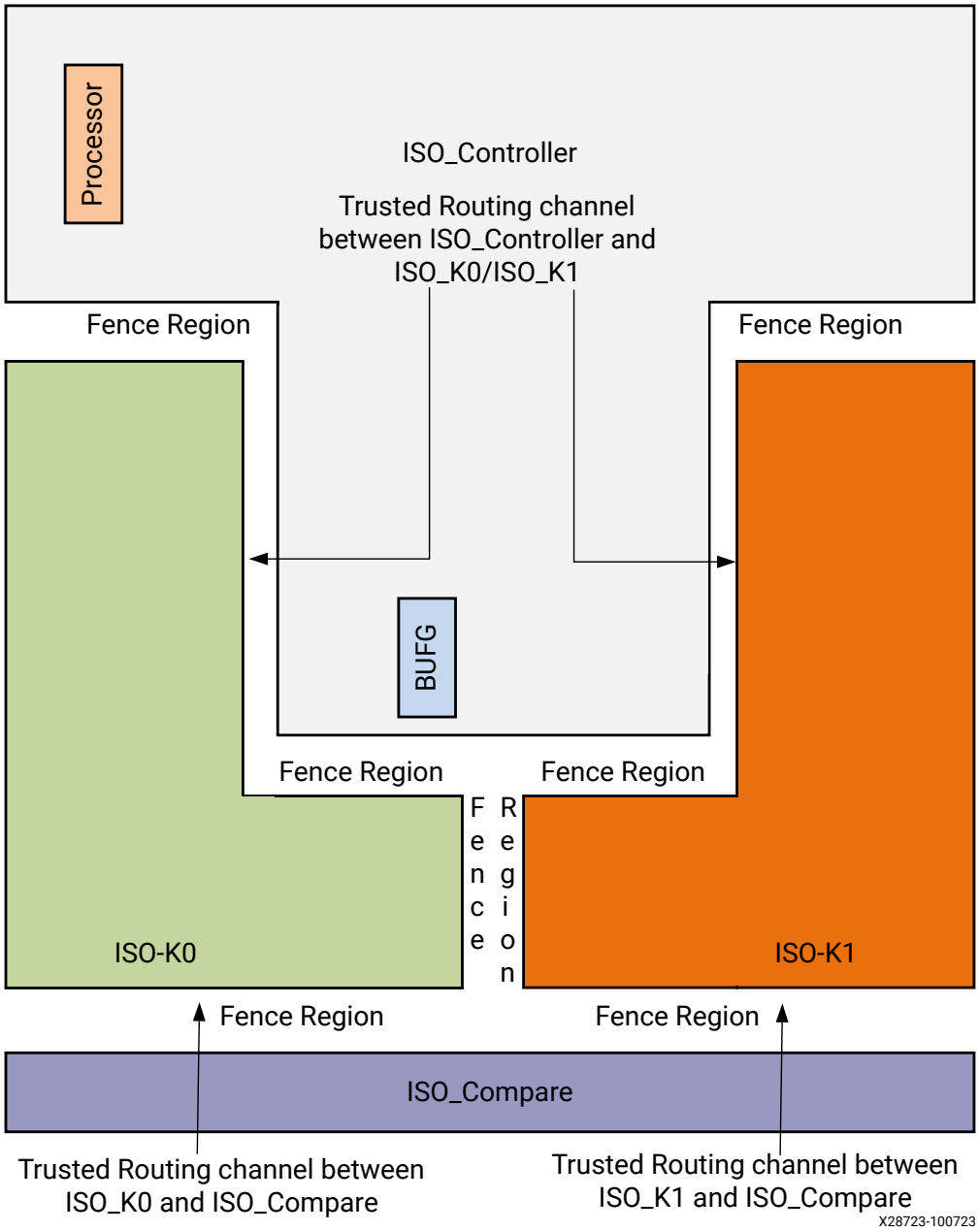
Figure 22: **Lab Flow Progression - System Floorplanning**



Floorplan Process

The floorplan of the reference design is shown in the following figure. Where inter-module communication (via Trusted Routing) is necessary, regions must be coincident with each other with a fence tile between the two intended regions.

Figure 23: **Floorplan of the Reference Design Highlighting the Trusted Routing Channels**



Floorplanning a design is the most time consuming part of the Isolation Design Flow. The purpose of this lab is not to test your skills in creating pblocks and placing pins, but to allow you to become familiar with the flow itself and how it integrates well in into IP integrator.

Scripts are provided that allow you to generate the floorplan in a few minutes rather than a few hours. Still, it is very important to understand the floorplanning rules and complexities that are associated with floorplanning any design (*Vivado Design Suite User Guide: Dynamic Function eXchange* (UG909) and *Vivado Design Suite User Guide: Hierarchical Design* (UG905). More details on the IDF rules are in *Isolation Design Flow for Xilinx 7 Series FPGAs or Zynq-7000 SoCs (Vivado Tools)* (XAPP1222).

1. Select the Tcl Console tab at the bottom of the Vivado GUI.
2. Enter the following commands:
   a. `cd c:/xilinx_design` (if not already in this directory)

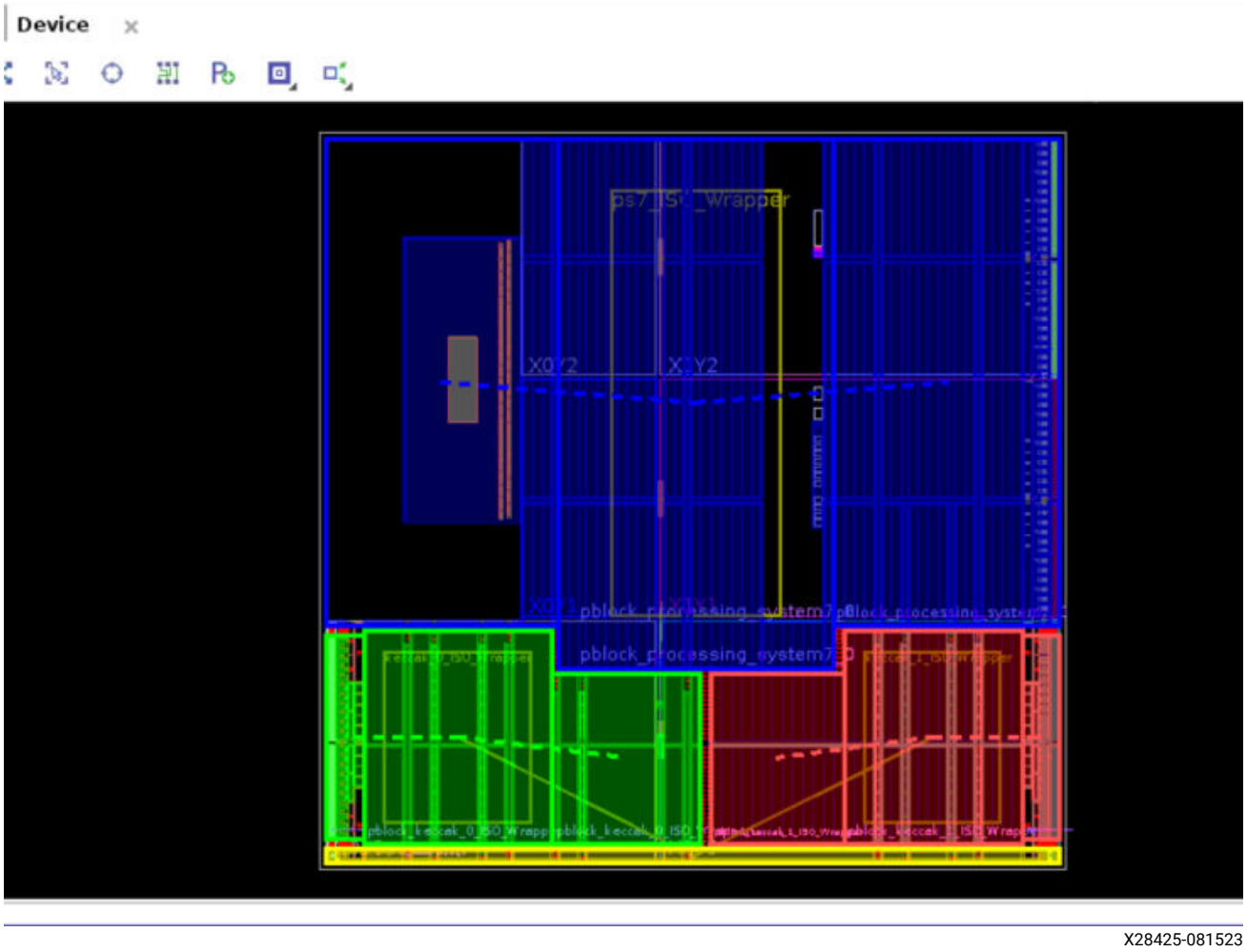
      ***Note*:** This assumes you extracted the lab design into `c:/xilinx_design`.

      ***Note*:** Make sure to use the Linux "/" instead of the Windows "\" when using the Vivado tool command language (Tcl) (see *Vivado Design Suite Tcl Command Reference Guide* (UG835) for more information).

   b. `source ./sources/xdc/pins.xdc`
   c. `source ./sources/xdc/k0.xdc`
   d. `source ./sources/xdc/k1.xdc`
   e. `source ./sources/xdc/compare.xdc`
   f. `source ./sources/xdc/controller.xdc`

   ***Note*:** There might be a warning for No Pblocks matched, which is due to the first XDC command in the file querying if the Pblock already exists. If so, delete it before creating a new Pblock.
3. Save the design, selecting **OK** and **YES**. When complete, your floorplan looks like the following figure.

Figure 24: **Completed Lab Design Floorplan**



X28425-081523

4. Save the design.

   An enhancement to IDF in Vivado is designed to allow global clocking components inside isolated modules. Global components cannot actually be isolated due to their global scope. Before IDF in Vivado, you had to modify their design and ensure such components were at the top level of their design. IDF in Vivado allows for attributes to be set to turn off isolation on them, allowing them to be nested but not isolated. This is particularly useful for clocks coming from the Zynq 7000 processing system (PS) region because they cannot be moved. In this design, all clocks and resets are generated by the PS region. To turn off isolation of the clocks, use the following command:

   ```
   set_property HD.ISOLATED_EXEMPT true [get_cells -hierarchical -
   filter {PRIMITIVE_TYPE =~ CLK.gclk.*}]
   ```

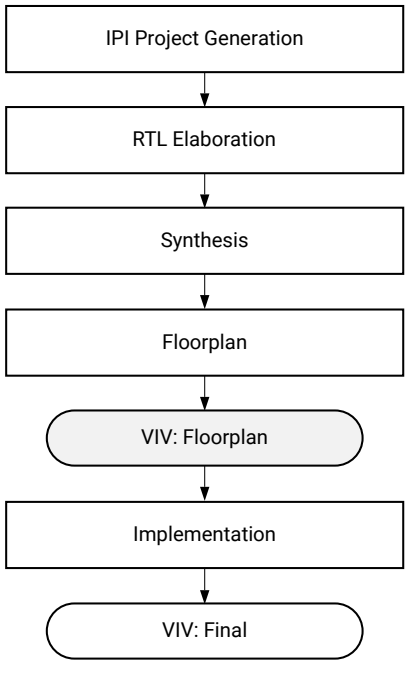
   In this example the `HD.ISOLATED_EXEMPT` property is applied globally to any and all clock components in your design. If your design has some clock components that you desire to be isolated, the safer method is to exempt only the ones in the processor block. This is accomplished by adding an additional item to the -filter option. The more restrictive filter option now looks as follows:

   ```
   -filter {NAME =~ *ps7* && PRIMITIVE_TYPE =~ CLK.gclk.*}
   ```

5. The new Tcl command is shown below. Enter the following statement in the Tcl Console window: `set_property HD.ISOLATED_EXEMPT true [get_cells -hierarchical - filter {NAME =~ *ps7* && PRIMITIVE_TYPE =~ CLK.gclk.*}]`
6. Save the design by selecting **OK** and **YES**.
7. Browse the floorplan around the fences, verifying the fence rules (no less than one user tile).

Running VIV Against the Floorplan

Figure 25: **Lab Flow Progression: VIV on Floorplan**



The AMD Vivado Isolation Verifier (VIV) software verifies that FPGA or SoC designs that have been partitioned into isolated modules meet the stringent standards for a fail-safe design. VIV is a Tcl script that runs in the Vivado tool framework in the form of DRCs. This allows for a strong GUI interface to the tool that was not available in the older ISE tools for IVT.

VIV is run on the floorplan to catch pin, I/O bank, and area group isolation faults early in the design, when changes are more easily integrated. The steps in this section guide you through the process. After implementation, the VIV is run against the routed design.

Constraint Checking (VIV - Constraints)

On the floorplan, VIV checks the following:

- Pins from different isolation groups are not physically adjacent, vertically or horizontally, at the die.

- Pins from different isolation groups are not physically adjacent at the package. Adjacency is defined in eight compass directions: north, south, east, west, northeast, southeast, northwest, and southwest.
- Pins from different isolation regions are not co-located in an I/O block (IOB) bank.

  ***Note*:** Though VIV does fault such conditions, only specific security-related applications require such bank isolation. The majority of applications allow for sharing of banks. Bank sharing is dependent on the specific application.
- The Pblock constraints in the XDC file are defined so that a minimum of a one tile wide fence exists between isolated regions.

Verifying the Floorplan with VIV

Enabling VIV DRC Checks

Vivado Isolation Verifier (VIV) 2.0 is used to run design rule checks (DRCs) for IDF flow. Refer to the *Vivado Isolation Verifier User Guide* (UG1291) for details on the DRCs.

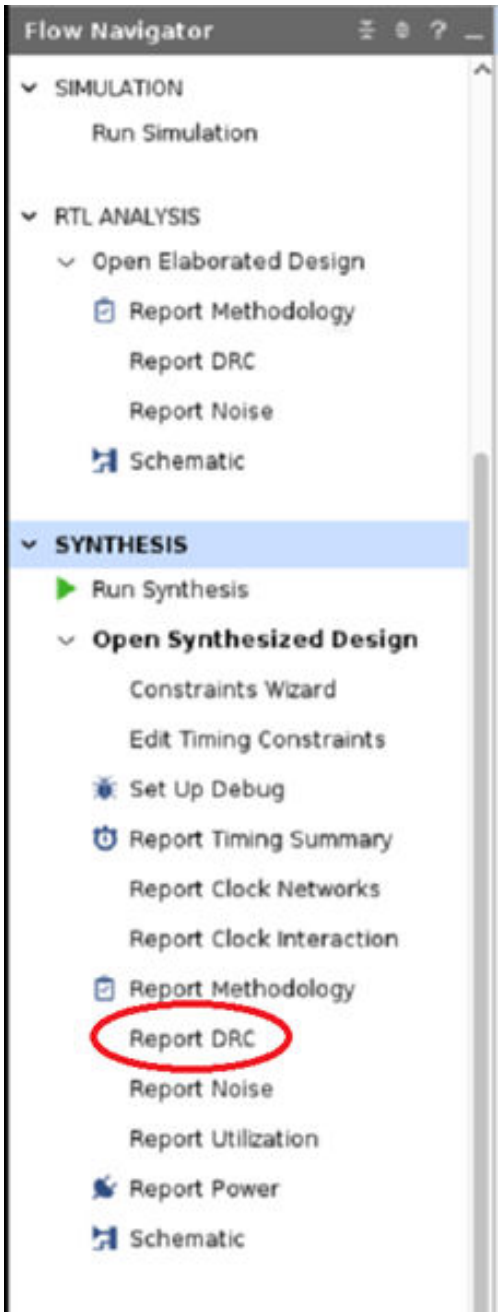
Enable VIV DRCs by running the following command from the TCL Console. `set_param hd.enableIDFDRC true`

IMPORTANT! *For Vivado versions 2021.1 and later the above step can be skipped as these later releases, the VIV DRCs are automatically enabled by the tool when it detects HD.ISOLATED set to true.*

1. If not already open, open the synthesized run by selecting Open Synthesized Design under the Synthesis section on the left of the Vivado GUI.

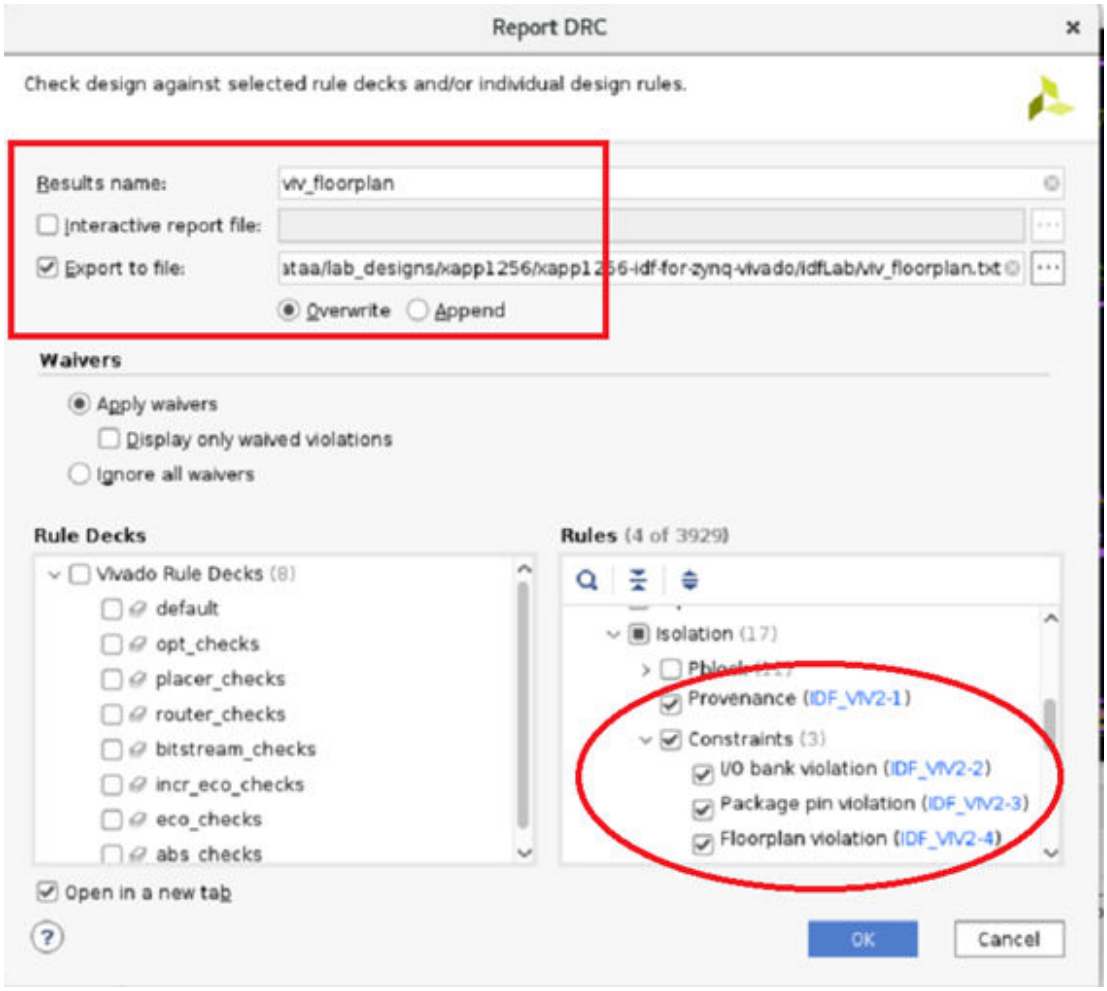
   ***Note*:** If the Open Synthesized Design option is not available, it is either already open or there is no Synthesis run available (requiring synthesis to be re-run).
2. Under the Synthesized Design pull-down of the Synthesis section, select Report DRC as shown in the following figure.

Figure 26: **Running DRCs after Synthesis**



3. Complete the following steps, as shown in the following figure.
   a. Uncheck all DRC rules (deselect All Rules).
   b. Expand all of the Isolation rules.
   c. Select IDF rules 1–4 (IDF Floorplan rules).
   d. Change the Results name field to viv_floorplan.
   e. Change the Output File field to `c:/xilinx_design/viv_floorplan.txt`.
   f. Click **OK**.

Figure 27: **VIV IDF Floorplan Rules (DRCs)**

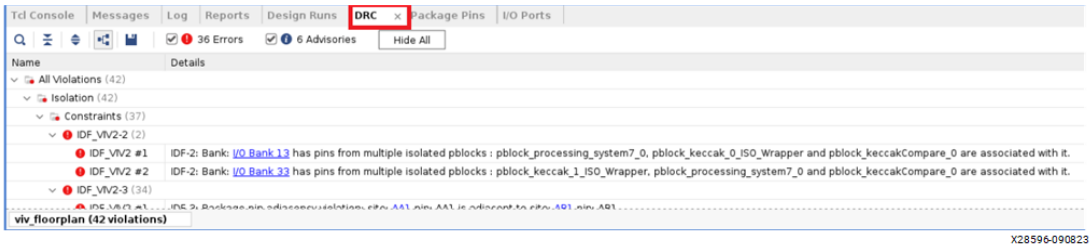


X28428-081523

4. All results are stored in the specified file (`c:/xilinx_design/viv_floorplan.txt`). For easier access, however, they are displayed in the DRC tab at the bottom of the Vivado GUI as shown in the following figure.

   ***Note*:** The DRC tab is only available after a DRC run has been executed.

Figure 28: **DRC Tab after VIV Floorplan Run**



X28596-090823

5. Inspect the results (42 violations are identified).

   a. IDF-1 (Provenance): IDF-1 documents the circumstances under which a DRC report was generated, including tool versions, date, design name, user, platform, and host. This DRC is informational. No errors are reported here.

b. IDF-2 (I/O bank violation): IDF-2 reports all I/O banks that have IOBs from more than one isolated region. Two I/O banks are used in this lab design and both contain IOBs from two distinct isolated regions, hence the two IDF-2 errors shown in the DRC run. I/O bank sharing is not an actual error. It is informational. There are some cases where I/O banks cannot be shared and some where they can. It depends on the user application and if that application allows a common I/O power supply between isolated regions.

c. IDF-3 (Package pin violation): IDF-3 reports errors where pins from different isolated regions are adjacent to each other at the package level. This lab has 31 pin adjacency errors. These are real errors and would be unacceptable for any design desiring physical isolation between such regions.

d. IDF-4 (Floorplan violation): IDF-4 reports all locations where one (or more) isolated region is either adjacent or overlaps another isolated region. There are no such violations in this design.

***Note*:** The DRC engine reports 42 violations, but only 36 can be accounted for. This discrepancy is due to the way the DRC engine counts violations. Any report (such as saying no violations found) increments the DRC rule violation counter. As such, the first missing violation is from IDF-1 where VIV outputs the provenance of the design, while the second missing violation is from IDF-4 reporting that no violations were found.

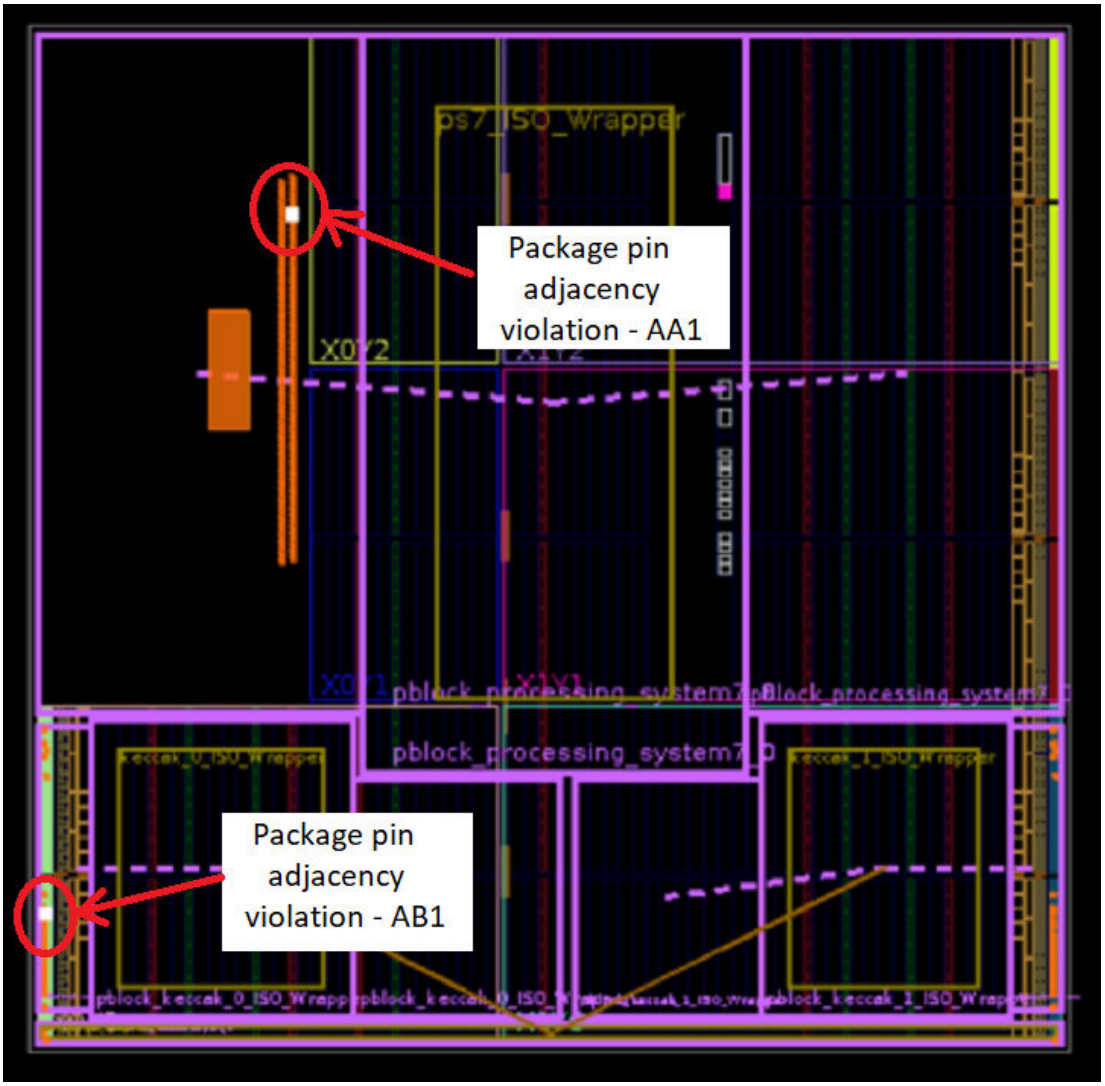
6. Select each violation as desired, and notice that the violation is highlighted in the Vivado GUI.

   ***Note*:** An example package pin adjacency violation (IDF-3), error IDF #1, is selected in the DRC tab. The corresponding device sites are highlighted in the GUI Device view, as shown in the following figure.

7. Select each violation as desired, and notice that the violation is highlighted in the Vivado GUI.

   ***Note*:** An example package pin adjacency violation (IDF-3), error IDF #1, is selected in the DRC tab. The corresponding device sites are highlighted in the GUI Device view, as shown in the following figure.

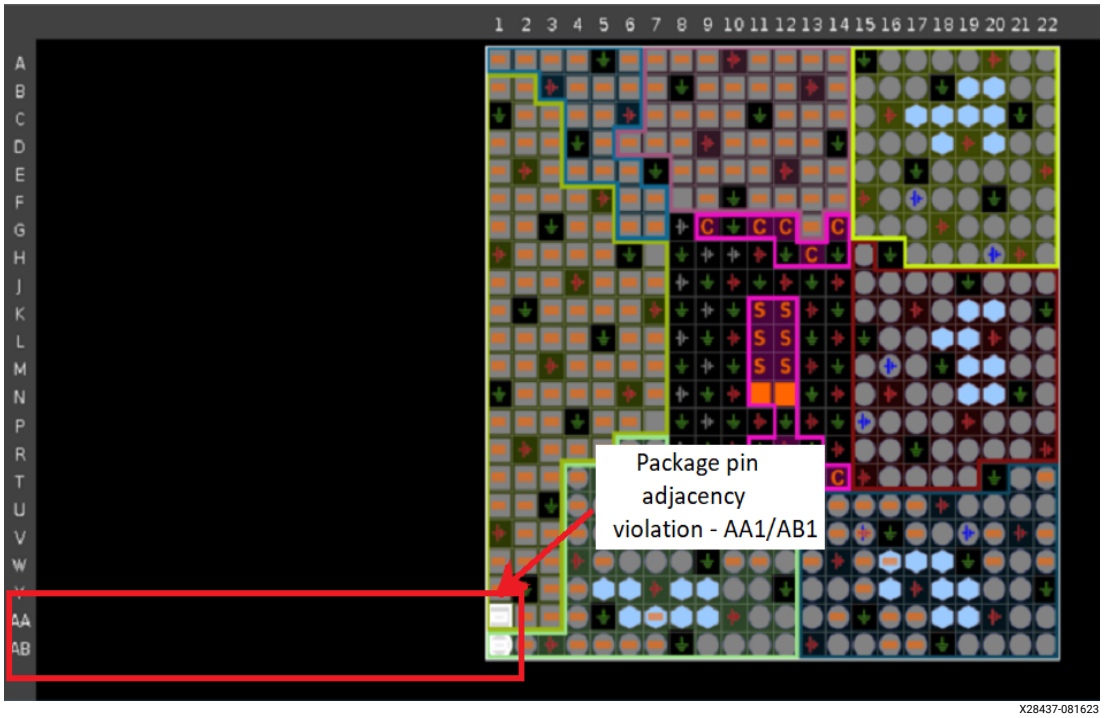
Figure 29: **Package Pin Adjacency Violation - Device View**



X28436-081623

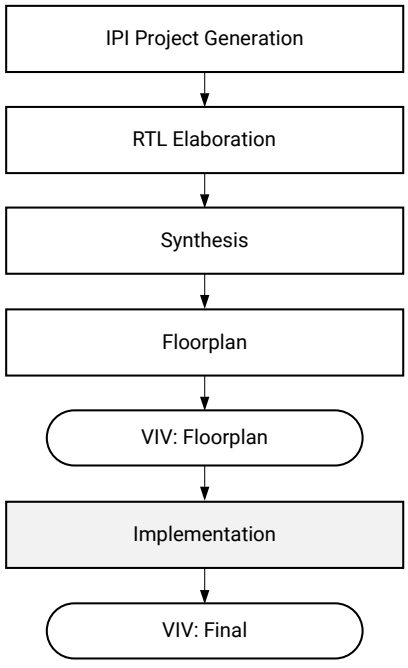
The corresponding pin adjacency violations for package pins AA1 and AB1 are highlighted in the GUI Package view as shown in the following figure. The Package view shows that these pins are indeed physically adjacent in the package.

Figure 30: **Package Pin Adjacency Violation - Package View**



Implementing the Design

Figure 31: **Lab Flow Progression - Implementation**



Generating and Running an Implementation

Implementing the Design

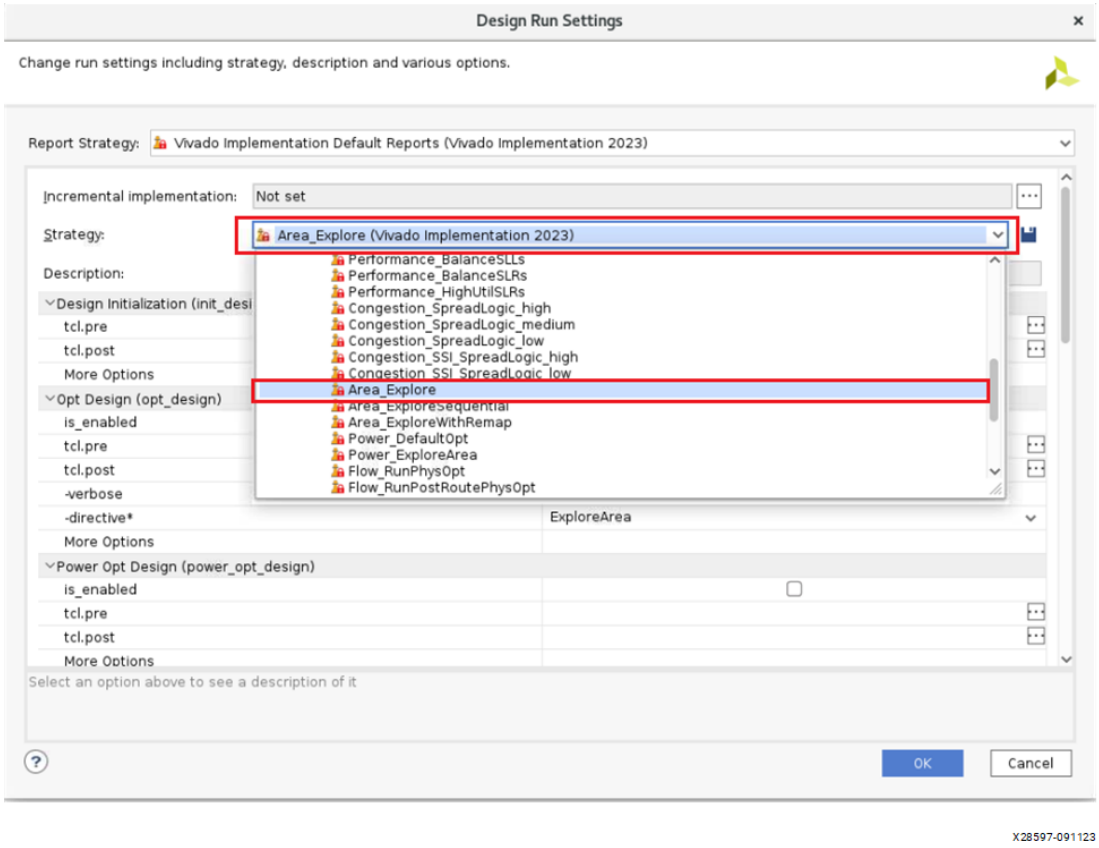
These steps describe how to generate and run a design implementation.

1. Under the Design Runs tab, at the bottom of the Vivado GUI, right-click *impl_1* and select *Change Run Settings*.
2. The lab design is densely populated for the K0 and K1 modules and the *Area Explore* run *Strategy* produces the best results.
   a. From the Stratagy pull-down menu, select *Area_Explore (Vivado Implementation 2023)*.

      ***Note*:** For other Vivado versions, please select corresponding Vivado Implementation option.

   b. Click **OK** (as shown in the following figure).

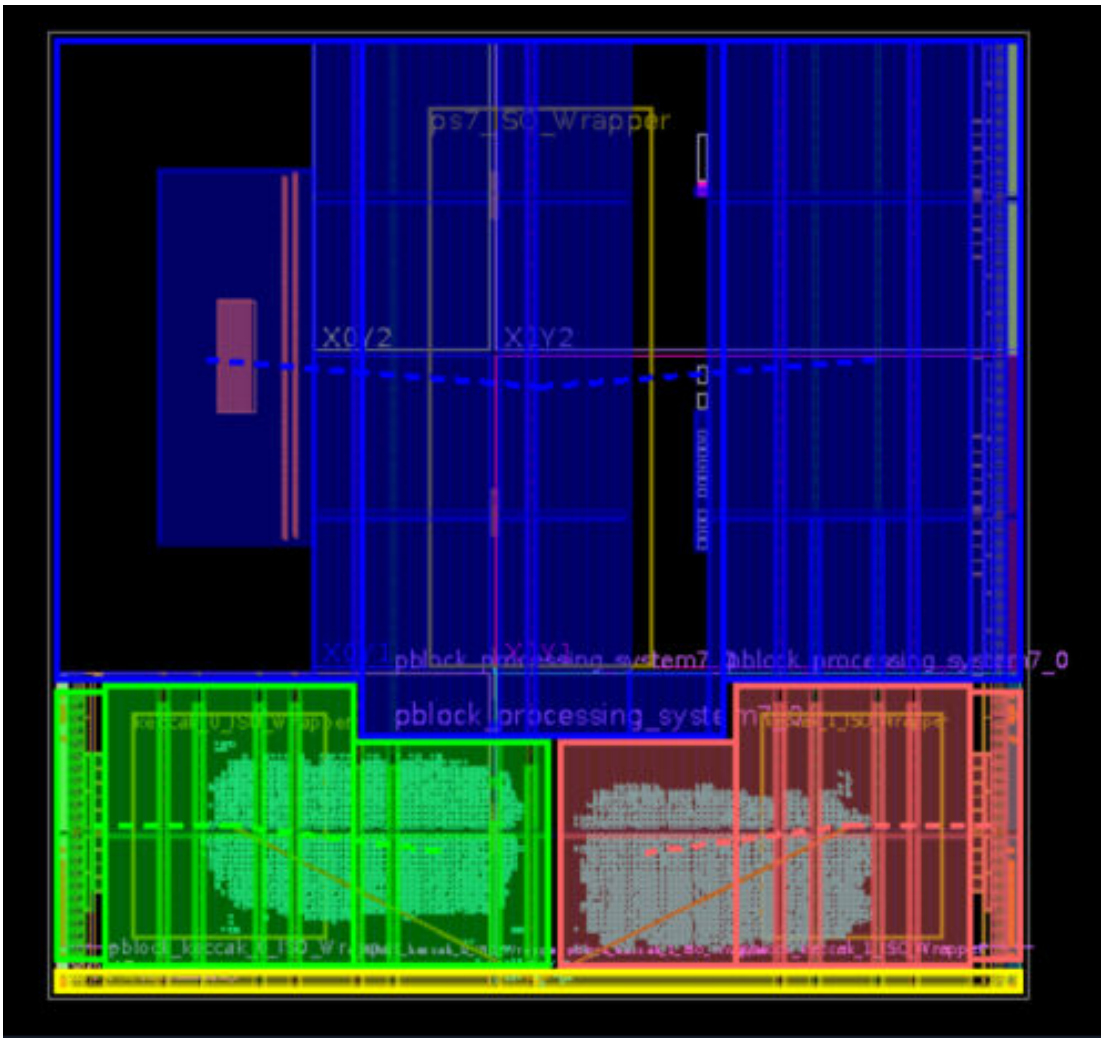
Figure 32: **Device View - Implemented Design**



3. Click **Run Implementation** under the Implementation menu on the left of the Vivado GUI.
4. Save the project or constraints if asked. If any constraints were modified, the Vivado tool requests starting from Synthesis. This is okay.
5. When implementation is complete, select the *Open Implemented Design* option and click **OK**. The device view will appear and look like the following figure (the pblocks are also highlighted to clearly identify the isolated regions).

6. If asked to close the Synthesized Design before opening the Implemented Design, click **Yes**. This is good practice because memory might be limited.

Figure 33: **Implemented Design - Device View**

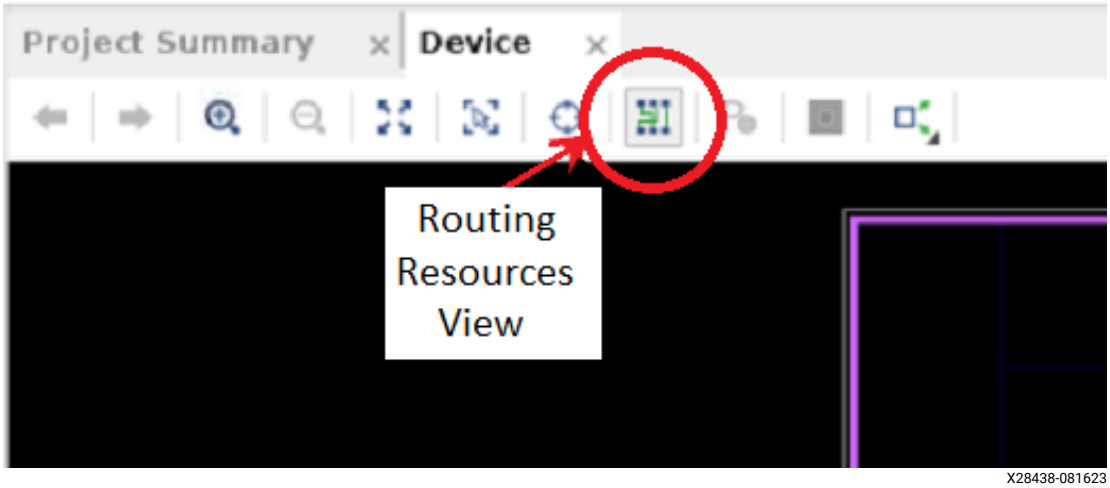


X28439-081723

Routing Resources View (Comments on the Mode)

These steps describe how to generate and run a design implementation.

Figure 34: **Enabling/Disabling Routing Resources Mode – Device View**



Gaps in the floorplan appear in this view because the tools do not consider the interconnect tiles associated with all user tiles as part of the pblock. This is visual only; the gaps do not exist.

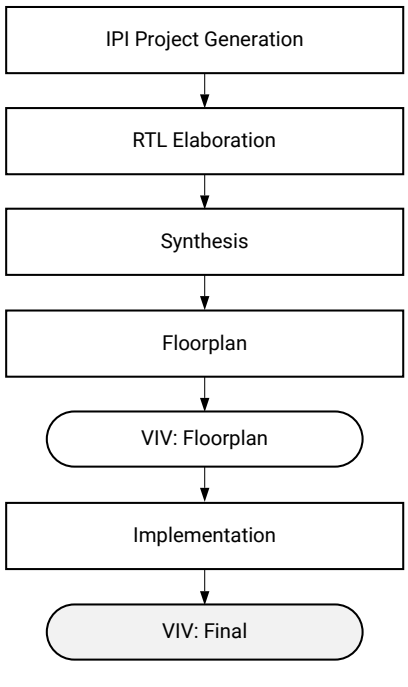
In this view, you can track a schematic net to the routed net. This is a very powerful view when tracing timing issues.

Also, from this view you can manually route any component or net as you wish. This mode is the Vivado replacement to the ISE FPGA Editor. The replacement is significantly more user friendly.

It is possible for routes, not touchdowns, from one isolated region to cross over into another isolated region if the region in question does not have any routing in that area. This allows for maximum flexibility to the router while still obeying IDF rules for isolation. This only happens in designs where sparsely populated isolated regions are adjacent to regions that are densely populated. No placement or touchdowns are ever allowed outside the intended isolated region.

Verifying the Routed Design with VIV

Figure 35: **Lab Flow Progression - VIV on Final Design**



VIV is run on the implemented design to catch isolation faults between isolated regions, as well as package pin and I/O bank violations (as when VIV was run on the floorplanned design). The steps in this section guide you through the process.

Final Isolation Verification (VIV - Implementation)

After the design is complete (placed and routed), VIV is used again on the implemented design to validate that the required isolation was built into the design.

At this step, VIV checks the following:

- VIV analyzes the complete placed and routed design.
- Tile-based isolation analysis looks for a barrier (fence) between isolated regions.
  - A valid user tile acts as a sufficient isolation barrier if:
    - It does not contain any isolated signals (from any isolated region).
    - It is configured in the default (unused) state.
- VIV does the same pin and I/O checking as in Floorplan mode.

Verifying the Implemented Design with VIV

Enabling VIV DRC Checks

Note: Vivado Isolation Verifier (VIV) 2.0 is used to run design rule checks (DRCs) for IDF flow. Refer to the *Vivado Isolation Verifier User Guide* (UG1291) for details on the DRCs. Enable VIV DRCs by running the following command from the TCL Console: `set_param hd.enableIDFDRC true`

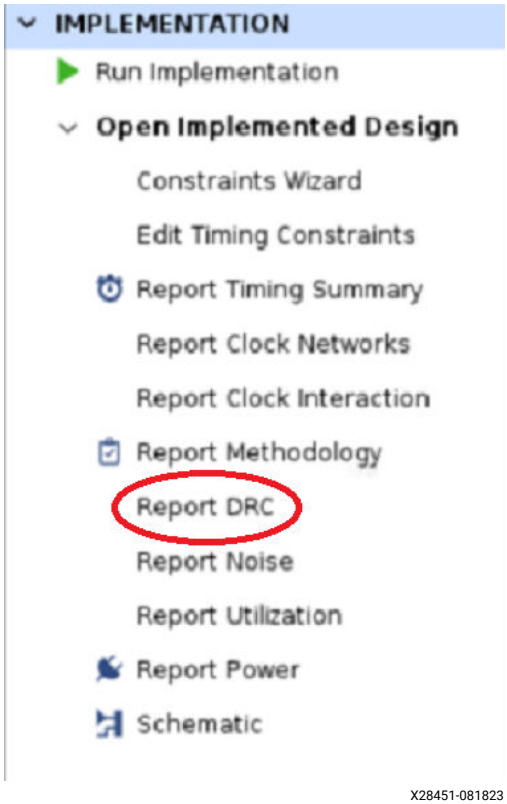
IMPORTANT! *For Vivado versions 2021.1 and later releases, skip ahead to Step 2. The VIV DRCs are automatically enabled by the tool when it detects* `HD.ISOLATED set to true`.

1. Open the implementation run from the Flow Navigator menu tree, if not already open. To open, expand *Implementation* from the tree and select *Open Implemented Design*. The Flow Navigator is located on the left side of the Vivado GUI.

   IMPORTANT! *If the option Open Implemented Design is not available, it is either already open or there is no Implementation run available (requiring implementation to be re-run).*

2. Under the Implemented Design expand the Implementation section from the menu tree, select Report DRC as shown in the following figure.

Figure 36: **Running DRCs after Implementation**



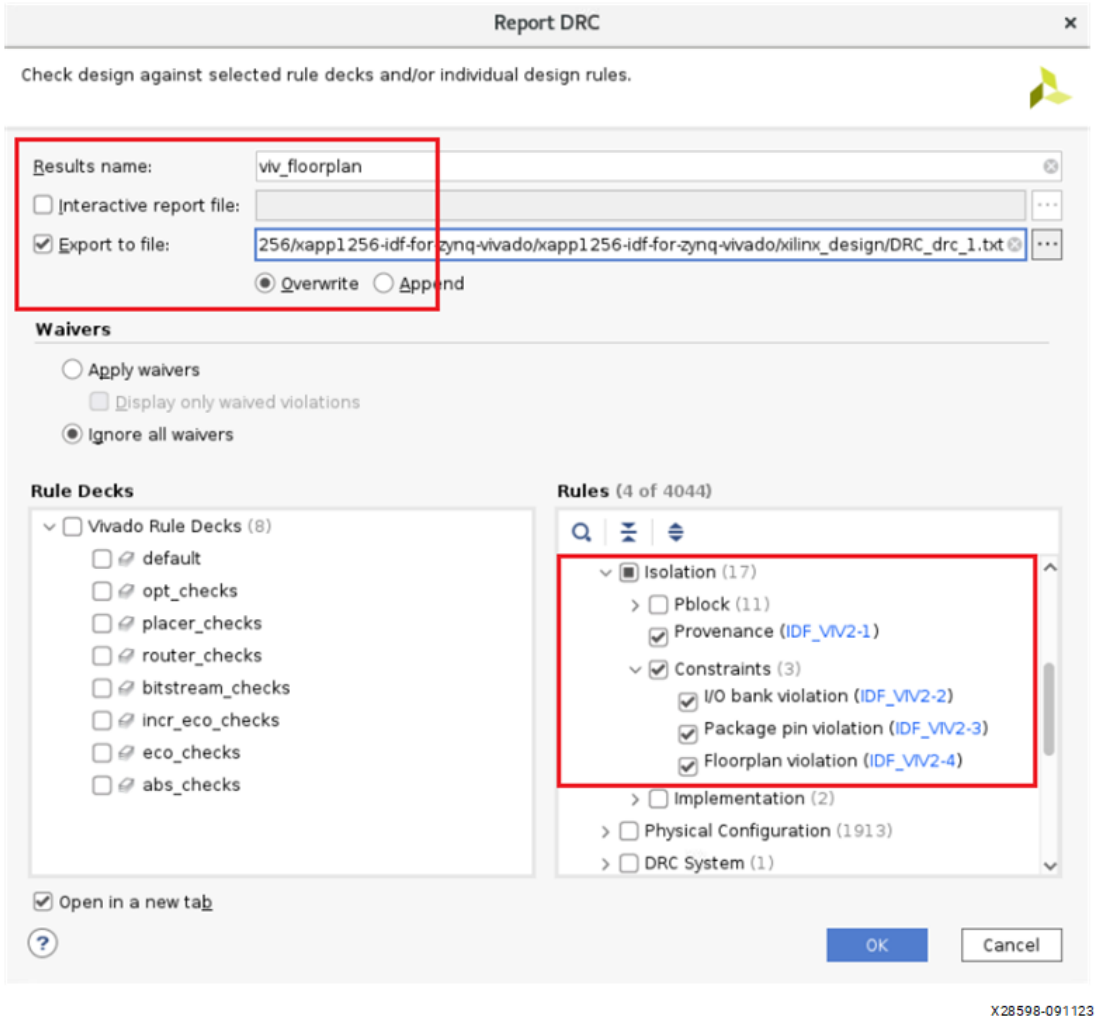
3. Complete the following steps, as shown in the following figure:
   a. Uncheck all DRC rules (deselect All Rules).
   b. Expand all of the Isolation rules.
   c. Select IDF rules 1–6 (IDF Floorplan rules).

d. Change the Results name field to viv_floorplan.

e. Change the Output File field to `c:/xilinx_design/viv_floorplan.txt`.

f. Select **OK**.

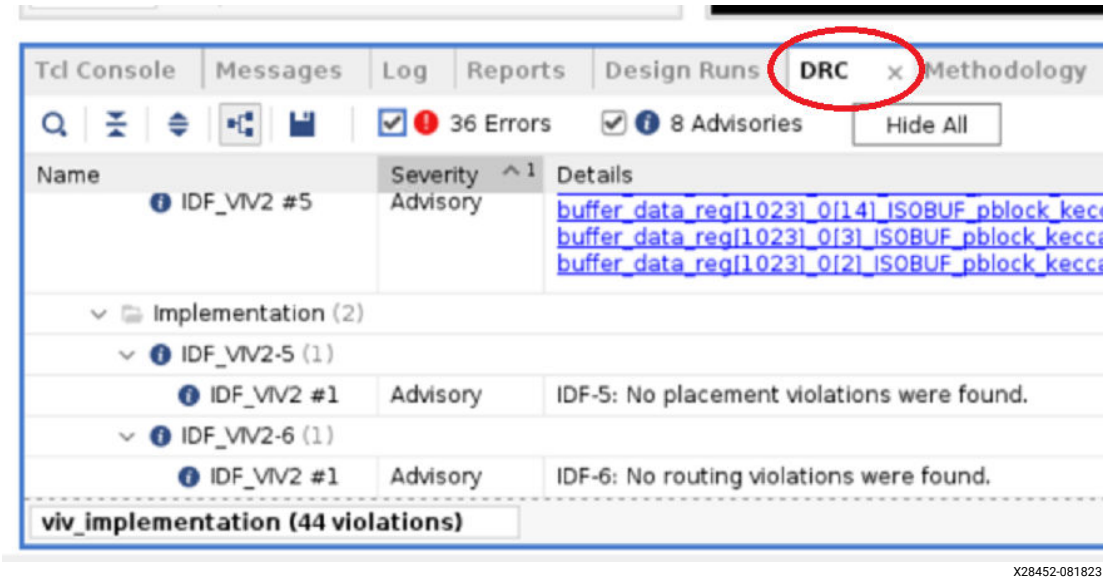
Figure 37: **VIV IDF Floorplan Rules (DRCs)**



4. All results are stored in the specified file (`c:/xilinx_design/viv_floorplan.txt`). For easier access, however, they are displayed in the DRC tab at the bottom of the Vivado GUI as shown in the following figure.

   ***Note*:** The DRC tab is only available after a DRC run has been executed.

Figure 38: **DRC Tab after VIV Floorplan Run**



5. Inspect the results (44 violations are identified).
    a. IDF-1 (Provenance): IDF-1 documents the circumstances under which a DRC report was generated, including tool versions, date, design name, user, platform, and host. This DRC is informational. No errors are reported here.
    b. IDF-2 (I/O bank violation): IDF-2 reports all I/O banks that have IOBs from more than one isolated region. Two I/O banks are used in this lab design and both contain IOBs from two distinct isolated regions, hence the two IDF-2 errors shown in the DRC run. I/O bank sharing is not an actual error. It is informational. There are some cases where I/O banks cannot be shared and some where they can. It depends on the user application and if that application allows a common I/O power supply between isolated regions.
    c. IDF-3 (Package pin violation): IDF-3 reports errors where pins from different isolated regions are adjacent to each other at the package level. This lab has 31 pin adjacency errors. These are real errors and would be unacceptable for any design desiring physical isolation between such regions.
    d. IDF-4 (Floorplan violation): IDF-4 reports all locations where one (or more) isolated region is either adjacent or overlaps another isolated region. There are no such violations in this design.
    e. IDF-5 (Placement violation): IDF-5 reports all placement violations. IDF-5 checks that no isolated logic or interconnect tile is adjacent to an isolated logic or interconnect tile of a different isolation group. There are no such violations in this design.
    f. IDF-6 (Routing violation): IDF-6 reports all routing violations and consists of three checks:
        i. All inter-region nets must have loads in exactly one isolated region.
        ii. No inter-region net can use nodes that have programmable interconnect points (PIPs) in the fence, except clock nets which can have unused PIPs in the fence.
        iii. For any tile containing inter-region nets, all such nets must have a common source and load.

    There are no such violations in this design.

***Note*:** Isolation groups are defined by Pblocks marked with the `HD.ISOLATED` property.

***Note*:** The DRC engine reports 44 violations, but only 36 can be accounted for. This discrepancy is due to the way the DRC engine counts violations. Any report (such as saying no violations found) increments the DRC rule violation counter. As such, the first missing violation is from IDF-1 where VIV outputs the provenance of the design, while the second, third, and fourth missing violations are from IDF-4, IDF-5, and IDF-6 reporting that no violations were found.

6. Select each violation as desired, and notice that the violation is highlighted in the Vivado GUI.

Conclusion

This application note provides a step-by-step example of how to implement a complete Zynq-7000 IDF design. All of the necessary IDF steps are shown, highlighting the rules and guidelines detailed in *Isolation Design Flow for Xilinx 7 Series FPGAs or Zynq-7000 SoCs (Vivado Tools)* (XAPP1222). This lab gives details on how functions are to be isolated, specific differences between a normal partition flow and a design using the IDF, information on IDF-specific HDL code mnemonics, and trusted routing rules. A designer wishing to create an IDF design should find all the necessary details using this application note and XAPP1222.

Reference Design Files

Download the Reference Design Files for this application note from the Xilinx website.

The reference design matrix in the following table indicates the tool flow and verification procedures used for the provided reference design.

Table 1: **Reference Design Matrix**

Parameter	Description
General	
Developer name	AMD
Target device	Zynq 7000 XC7Z020
Source code provided	Yes
Source code format	VHDL
Design uses code or IP from existing reference design, application note, third party, or Vivado software? If yes, list.	No
Simulation	
Functional simulation performed?	Yes
Timing simulation performed?	Yes
Test bench used for functional and timing simulations?	Yes
Test bench format	VHDL
Simulator software and version used	Vivado Design Suite 2023.1
SPICE/IBIS simulations?	No
Implementation	
Implementation software tools and versions used	Vivado Design Suite 2023.1
Static timing analysis performed?	Yes

Table 1: **Reference Design Matrix** *(cont'd)*

Parameter	Description
Hardware Verification	
Hardware verified?	No
Hardware platform used for verification	N/A

References

These documents provide supplemental material useful with this guide:

1. *7 Series Isolation Design Flow Lab Using ISE Design Suite 14.4* (XAPP1085)
2. Isolation Design Flow website
3. *Isolation Design Flow for Xilinx 7 Series FPGAs or Zynq-7000 SoCs (Vivado Tools)* (XAPP1222)
4. *Vivado Isolation Verifier User Guide* (UG1291)
5. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
6. *Vivado Design Suite User Guide: Dynamic Function eXchange* (UG909)
7. *Vivado Design Suite User Guide: Hierarchical Design* (UG905)
8. *Vivado Design Suite Tcl Command Reference Guide* (UG835)
9. Aerospace and Defense Security Monitor IP Core Product Marketing Brief

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
10/20/2023 Version 1.2	
Creating an IP Integrator Block Design	Updated Step 8.c. connection from data0_valid to data1_valid.
Verifying the Floorplan with VIV	Removed Step 1.
Implementing the Design	Updated Vivado Implementation to 2023.
Verifying the Routed Design with VIV	Removed Step 1.
03/21/2016 Version 1.1.1	
Throughout Document	Updated the title to clarify support for 7 series FPGAs.
02/24/2016 Version 1.1	
Verifying the Floorplan with VIV	Updated the title, Figure 28, and Figure 38.
03/21/2016 Version 1.0	
Initial Xilinx release.	N/A

Please Read: Important Legal Notices